The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The MOS Memory Data Book

for Design Engineers

1980

TEXAS INSTRUMENTS
INCORPORATED

ALPHANUMERIC INDEX, TABLE OF CONTENTS, SELECTION GUIDE, U.S. SALES OFFICES & AUTHORIZED DISTRIBUTORS — REFERENCE

INTERCHANGEABILITY GUIDE — INTERCHANGEABILITY GUIDE

DYNAMIC RAM DATA SHEETS — DRAMs

STATIC RAM DATA SHEETS — SRAMs

EPROM DATA SHEETS — EPROMs

ROM DATA SHEETS — ROMs

MEMORY SYSTEMS DATA SHEETS — MEMORY SYSTEMS

MECHANICAL DATA — MECHANICAL DATA

MANUFACTURING FLOW — MANUFACTURING FLOW

TESTING/RELIABILITY — TESTING/ REL

GLOSSARY/TIMING CONVENTIONS/DATA SHEET STRUTURE — GLOSSARY

LOGIC SYMBOLS — LOGIC

Texas Instruments, Inc.
MOS Memory Division, M/S 6965
P.O. Box 1443
Houston, Texas 77001

The MOS Memory Data Book

for

Design Engineers

1980

TEXAS INSTRUMENTS
INCORPORATED

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(Numbers in parentheses indicate overall complexity)

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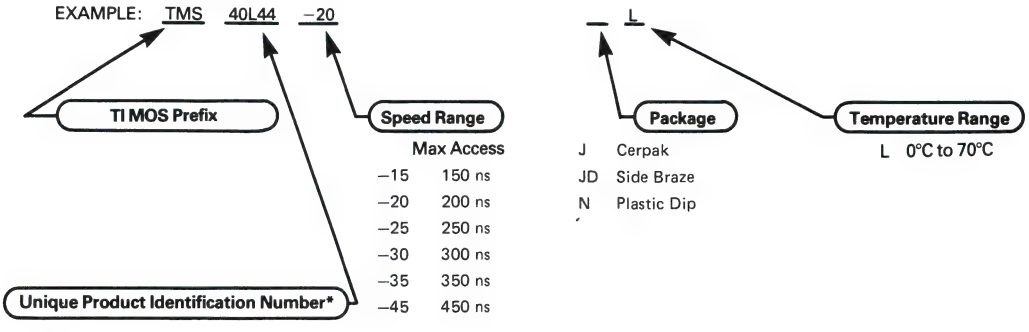
INTERCHANGEABILITY GUIDE

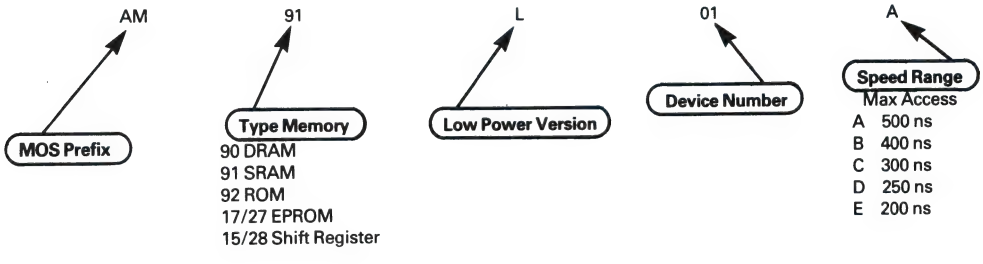
PART I — ALTERNATE VENDOR PART NUMBERING (EXAMPLES)

TEXAS INSTRUMENTS (TI)

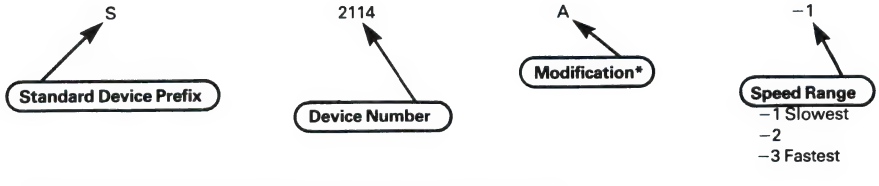


* L indicates low power

ADVANCED MICRO DEVICES (AMD)

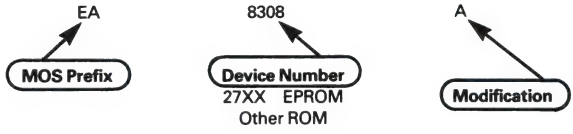


AMERICAN MICROSYSTEMS, INC. (AMI)

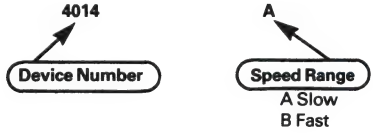


*Can also be "L", usually indicates lower power and/or improved speed

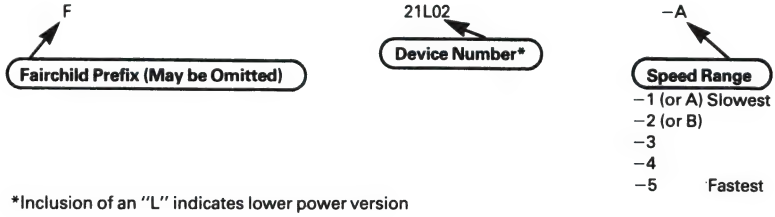
ELECTRONIC ARRAYS, INC (EA)



EMM/SEMI

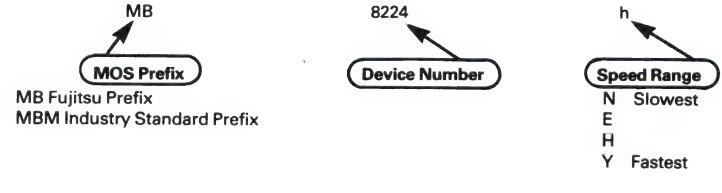


FAIRCHILD



*Inclusion of an "L" indicates lower power version

FUJITSU



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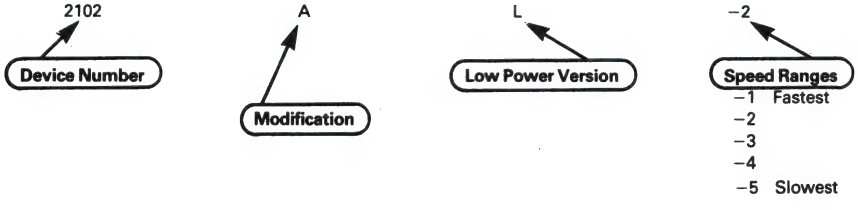
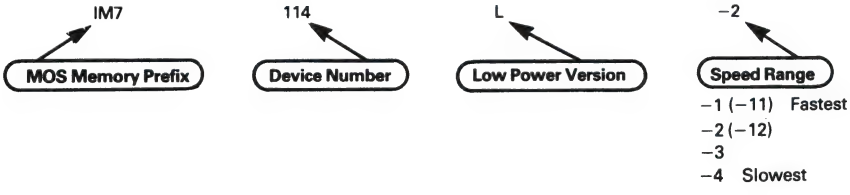
HITACHI

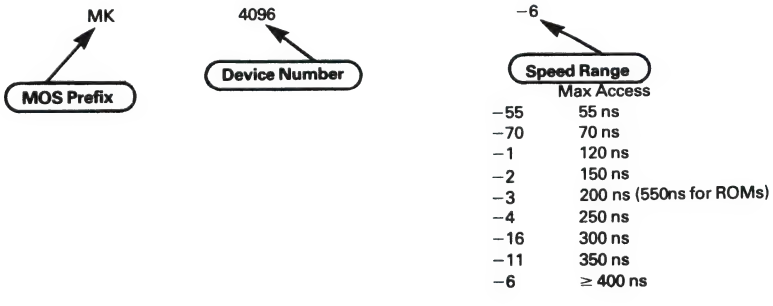
INTEL



INTERSIL/AMS

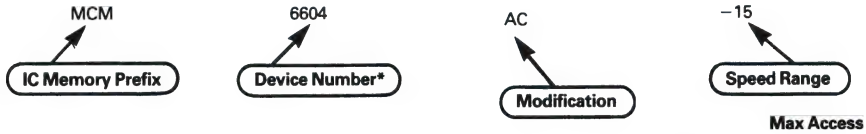


MOSTEK



INTERCHANGEABILITY GUIDE

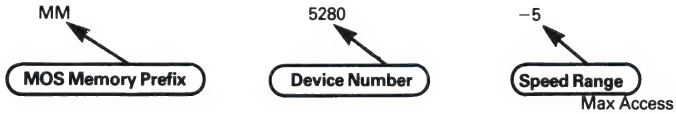
MOTOROLA



	Max Access
−2 (−15)	150 ns
−3 (−20)	200 ns
−4 (−25)	250 ns
−5 (−30)	300 ns
−11	350 ns
−6 (−45)	450 ns

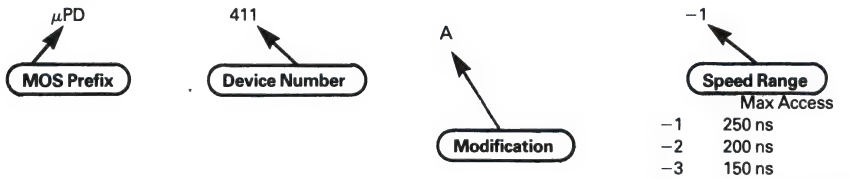
*** Inclusion of an "L" indicates low power version**

NATIONAL SEMICONDUCTOR



	Max Access
−1	500 ns
−2	650 ns
−4	450 ns
−5	270 ns

NIPPON ELECTRIC CORPORATION (NEC)



	Max Access
−1	250 ns
−2	200 ns
−3	150 ns
−4	135 ns (DRAMs) 450 ns (SRAMs)

SIGNETICS

−3	Fastest
−1	
−2	Slowest

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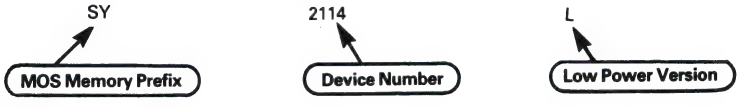
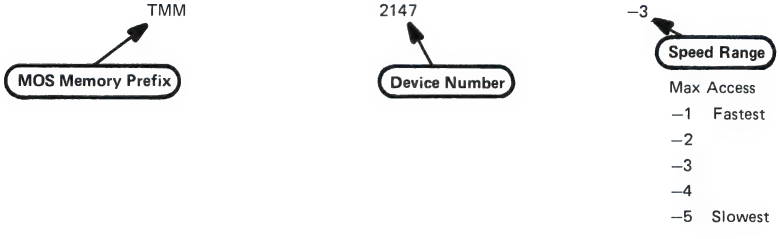
SYNERTEK



TOSHIBA



PART II – SECOND SOURCES*

* Based on available published data. (Official second sourcing agreements not necessarily implied.)
All devices listed operate over the 0°C to 70°C temperature range.

DYNAMIC RAMS

		VENDOR	PART NUMBER
8K X 1	Left Array (0), Right Array (1)	TI	TMS 4108-20 NL0 or NL1
	Second Sources	Mostek	MK 4108-40 or 41
16K X 1		TI	TMS 4116
	Second Sources	Fairchild	F 16K
		Fujitsu	MB 8116
		Hitachi	HM 4716
		Intel	2117
		Intersil	IM 7116
		ITT	4116
		Mostek	MK 4116
		Motorola	MCM 4116
		National	MM 5290
		NEC	μPD 416
		Toshiba	TMM 416
64K X 1	5 V	TI	TMS 4164
	Second Sources	Motorola	MCM 6664

STATIC RAMS

		VENDOR	PART NUMBER
4K X 1	Max Access ≥ 150 ns	TI	TMS 4044/TMS 40L44
	Second Sources	Intersil	IM 7141/IM 7141L
		National SC	MM 5257/MM 5257L
1K X 4	Max Access ≥ 150 ns	TI	TMS 2114/TMS 2114L
	Second Sources	AMD	AM 9114/AM 91L14
		AMI	S2114/S2114L/S2114A
		EMM/SEMI	2114
		Fujitsu	MB 8114
		Hitachi	HM 472114
		Intel	2114/2114L
		Intersil	IM 7114/IM 7114L
		National SC	MM 2114/MM 2114L
		NEC	μPD 2114L
		Synertek	SY 2114/SY 2114L
4K X 1	Max Access ≥ 55 ns	TI	TMS 2147/TMS 21L47
	Second Sources	AMD	AM 9147
		AMI	S2147
		Fujitsu	MBM 2147
		Hitachi	HM 6147/HM 6147L
		Intel	2147/2147L
		Mostek	MK 2147
		Motorola	MCM 2147
		National SC	MM 2147
		NEC	μPD 4104
		Toshiba	TMM 2147

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STATIC RAMS (continued)

		VENDOR	PART NUMBER
1K X 8	Max Access 450 ns	TI	TMS 4008
	Second Sources	Anticipated in 1980	
2K X 8	Max Access ⩾ 150 ns	TI	TMS 4016
	Second Sources	Toshiba	TC 5516P

EPROMS

		VENDOR	PART NUMBER
1K X 8	Max Access 350 ns/450 ns	TI	TMS 2708/TMS 27L08
3 Supply	Second Sources	AMD	AM 2708
		EA	EA 2708
		Fairchild	2708
		Fujitsu	MB 8518H
		Hitachi	HN 462708
		Intel	2708/2708L
		Motorola	MCM 2708
		National SC	MM 2708
		Signetics	2708
1K X 8	Max Access ⩾ 250 ns	TI	TMS 2508
5 V	Second Sources	Anticipated in 1980	
1K X 8	Max Access 450 ns	TI	TMS 2758
5 V	Second Sources	Intel	2758
2K X 8	Max Access 450 ns	TI	TMS 2716
3 Supply	Second Sources	Motorola	
2K X 8	Max Access 350 ns/450 ns	TI	TMS 2516
5 V	Second Sources	AMD	2716
		AMI	S4716
		Fujitsu	MBM 2716
		Hitachi	HN 462716
		Intel	2716
		Mostek	MK 2716
		Motorola	MCM 2716A
		National	MM 2716
		NEC	μPD 2716
		Signetics	2716
		Synertek	SY 2716
		Toshiba	TMM 323
4K X 8	Max Access 450 ns	TI	TMS 2532/TMS 25L32
5 V	Second Sources	Hitachi	HN 462732
		Motorola	MCM 2532
8K X 8	Max Access 450 ns	TI	TMS 2564
5 V	Second Sources	Anticipated in 1980	

DYNAMIC RAM DATA SHEETS

TMS 4108 NL
8,192-BIT DYNAMIC RANDOM-ACCESS MEMORY

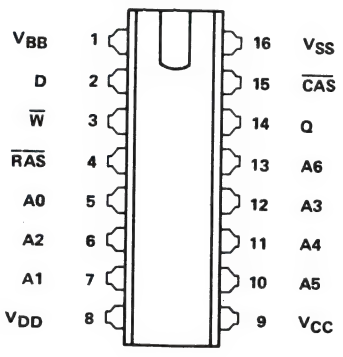
AUGUST 1979

- 8,192 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL-Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4108-15	150 ns	100 ns	375 ns	375 ns
TMS 4108-20	200 ns	135 ns	375 ns	375 ns
TMS 4108-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - Operating . . . 462 mW (max)
  - Standby . . . 20 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7,62 mm) Package Configuration

16-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE			
A0-A6	Address Inputs	$\overline{W}$	Write Enable
$\overline{CAS}$	Column address strobe	V_{BB}	−5-V power supply
D	Data input	V_{CC}	+5-V power supply
Q	Data output	V_{DD}	+12-V power supply
$\overline{RAS}$	Row address strobe	V_{SS}	0 V ground

description

The TMS 4108 series is composed of monolithic high-speed Dynamic 8,192-bit MOS random-access memories organized as 8,192 one-bit words and employing single-transistor storage cells and N-channel silicon-gate technology.

All input and outputs are compatible with Series 74 TTL circuits including clocks, Row Address Strobe ($\overline{RAS}$ or R), and Column Address Strobe ($\overline{CAS}$ or C). All address lines (A0 through A6) and the data input (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

There are two array-select versions of the TMS 4108, each offered in the three speed ranges indicated above and in plastic (NL suffix) packaging only. The left-array version is indicated by "0" following the type number (e.g., TMS 4108-15 NL0), and the right-array version is indicated by "1" (e.g., TMS 4108-25 NL1). Each 8K X 1 version is in a 16-pin dual-in-line package rated for operation from 0°C to 70°C.

operation

address (A0 through A6)

Thirteen address bits are required to decode 1 of 8,192 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). If the type number is followed by a "0", then column address input A0 must always be at V_{IL}; if it is followed by a "1", column address A0 must always be at V_{IH}. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

†The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

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PRELIMINARY DATA SHEET:
Supplementary data will be published at a later date.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode, and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$-only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

page mode

Page-mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to set up and strobe sequential row addresses on the same page is eliminated. To extend beyond the 64 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 8K RAMs. $\overline{CAS}$ is decoded to select the proper RAM.

power-up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

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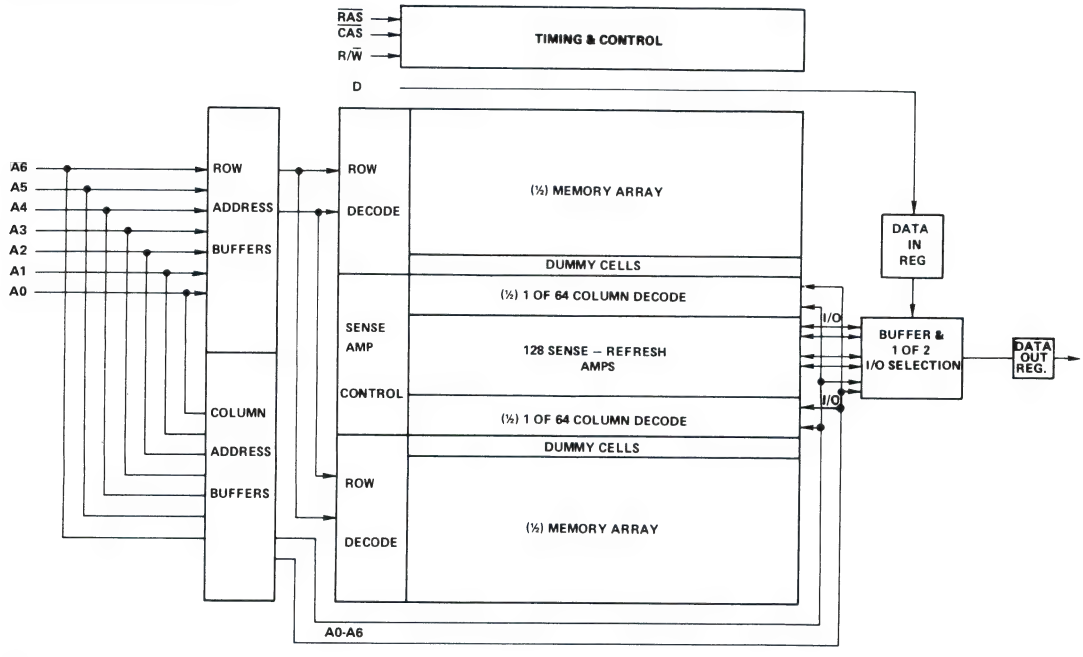
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin (see Note 1)	−0.5 to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS}	−1 to 15 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}		−4.5	−5	−5.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7	
Low-level input voltage, V_{IL}		−1†	0	0.8	V
Refresh time, $t_{refresh}$				2	ms
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention where the more negative limit is designated as minimum is used in this data sheet for logic voltage levels and time intervals.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V			±10	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}$ high			±10	μA
I_{BB1}	Average operating current during read or write cycle	Minimum cycle time		50	200	μA
I_{CC1}*					4	mA
I_{DD1}				27	35	mA
I_{BB2}	Standby current	After 1 memory cycle $\overline{RAS}$ and $\overline{CAS}$ high		10	100	μA
I_{CC2}					±10	μA
I_{DD2}				0.5	1.5	mA
I_{BB3}	Average refresh current	Minimum cycle time $\overline{RAS}$ cycling, $\overline{CAS}$ high		50	200	μA
I_{CC3}					±10	μA
I_{DD3}				20	27	mA
I_{BB4}	Average page-mode current	Minimum cycle time $\overline{RAS}$ low, $\overline{CAS}$ cycling		50	200	μA
I_{CC4}*					4	μA
I_{DD4}				20	27	mA

*V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading. Output loading is two standard TTL loads.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALTERNATE SYMBOL	TMS 4116-15		TMS 4116-20		TMS 4116-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from row address strobe	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200		250	ns
t_{PXZ}	Output disable time	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

†All typical values are at T_A = 25°C and nominal supply voltages.

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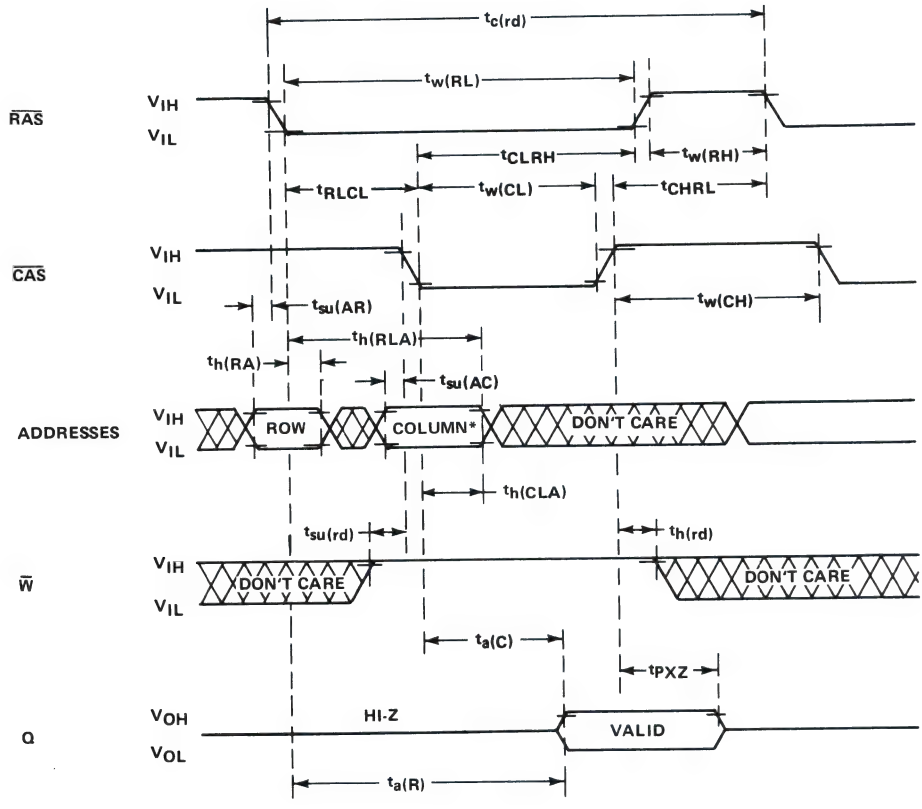
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALTERNATE SYMBOL	TMS 4108-15		TMS 4108-20		TMS 4108-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	170		225		275		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(RW)}$	Read-modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse width, column address strobe high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse width, column address strobe low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse width, row address strobe high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse width, row address strobe low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		75		ns
t_T	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	35	3	50	3	50	ns
$t_{su(AC)}$	Column address setup time	t_{ASC}	−10†		−10†		−10†		ns
$t_{su(AR)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(CLA)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(RA)}$	Row address hold time	t_{RAH}	20		25		35		ns
$t_{h(RLA)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(RLC)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	150		200		250		ns
$t_{h(CLD)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		75		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(WLD)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		75		ns
$t_{h(rd)}$	Read command hold time	t_{RCH}	0		0		0		ns
$t_{h(CLW)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(RLW)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{CHRL}	Delay time, column address strobe high to row address strobe	t_{CRP}	−20†		−20†		−20†		ns
t_{CLRH}	Delay time, column address strobe low to row address strobe high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, column address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{CWD}	70		95		125		ns
t_{rf}	Refresh time interval	t_{REF}		2		2		2	ms
t_{RLCL}	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, row address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, $\overline{W}$ low to column address strobe low (early write cycle)	t_{WCS}	−20†		−20†		−20†		ns

†The algebraic convention where the more negative limit is designated as minimum is used on this data sheet for logic voltage levels and time invervals.

read cycle timing



*For Column Address:
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

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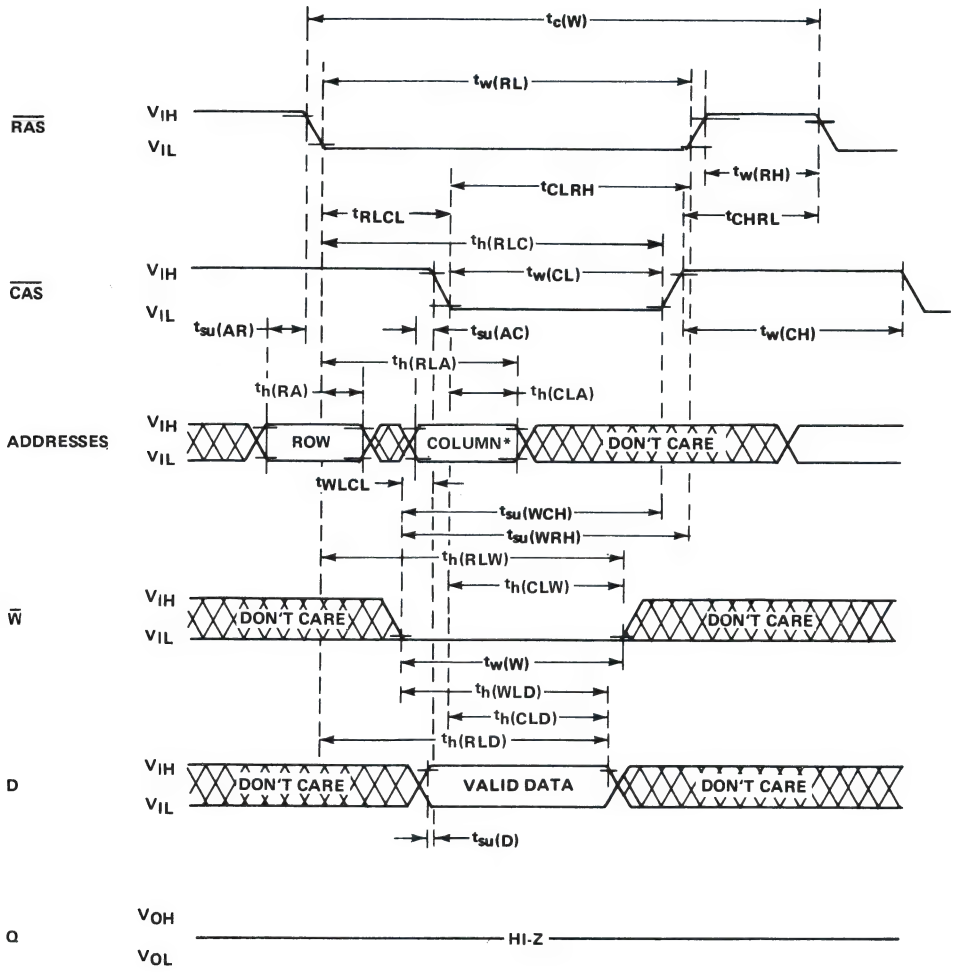
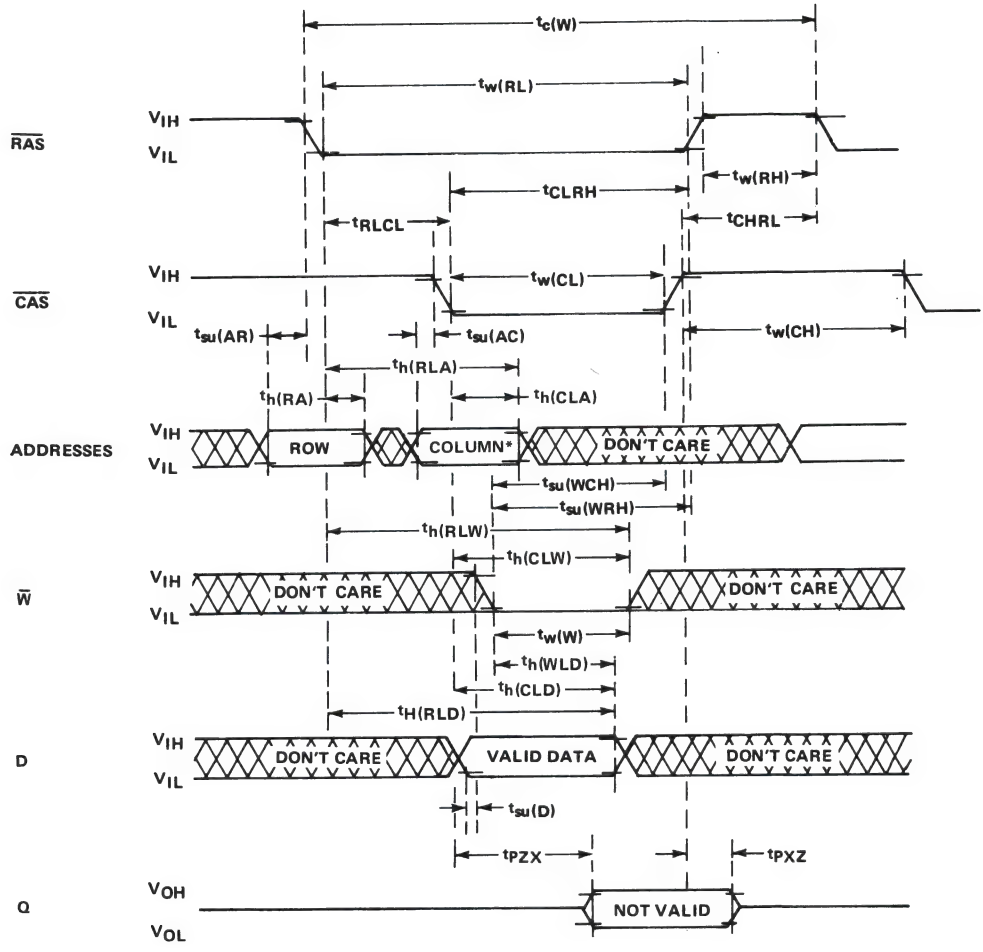
early write cycle timing



*For Column Address:
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

write cycle timing



*For Column Address:
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

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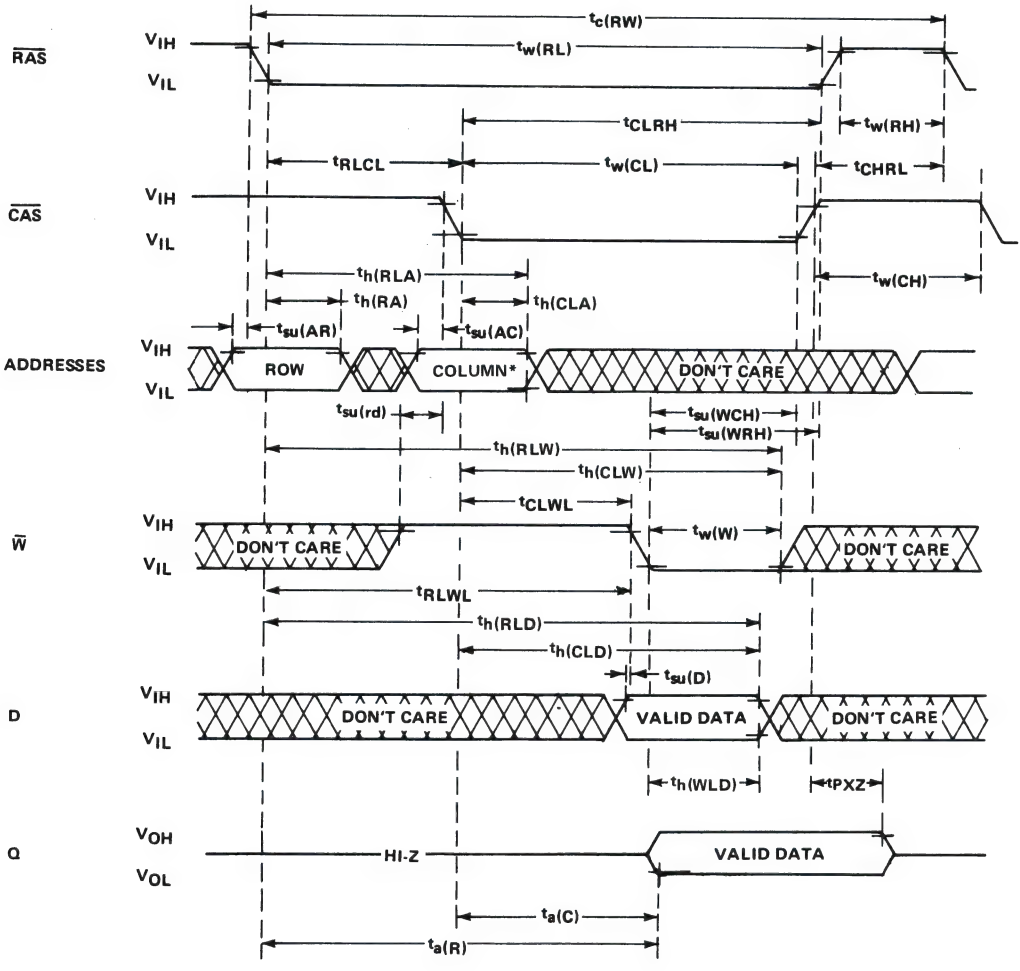
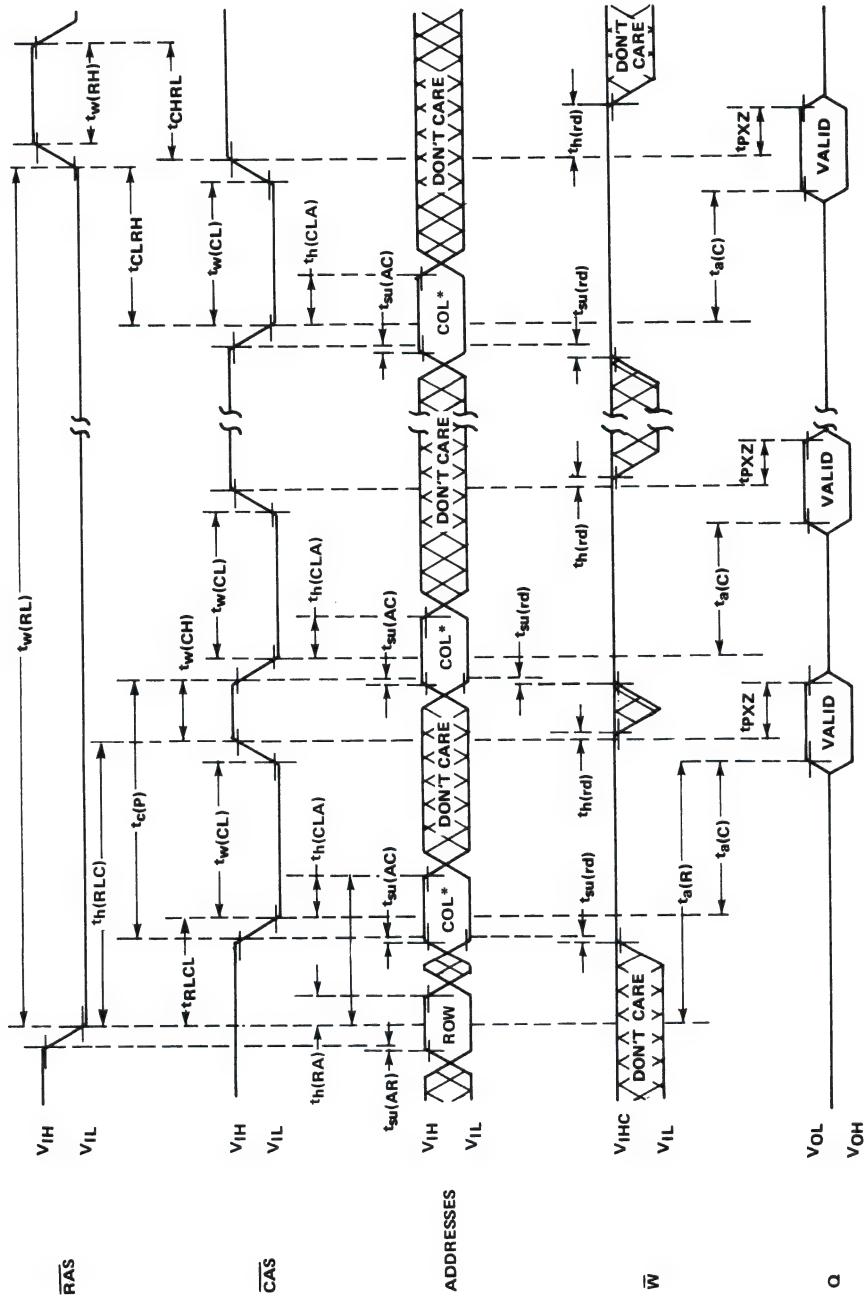
read-write/read-modify-write cycle timing



*For Column Address:
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

page-mode read cycle timing



*For Column Address
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

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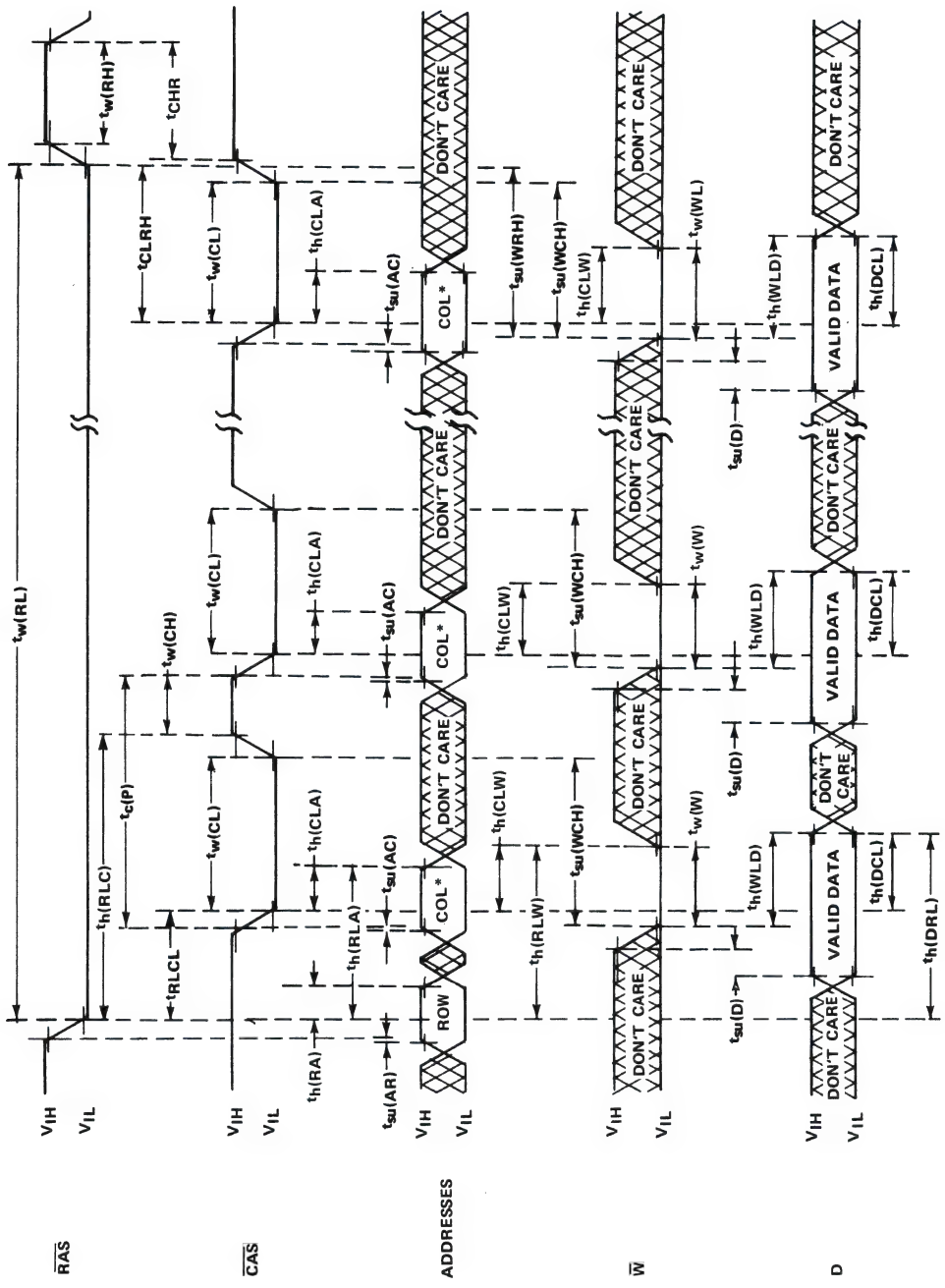
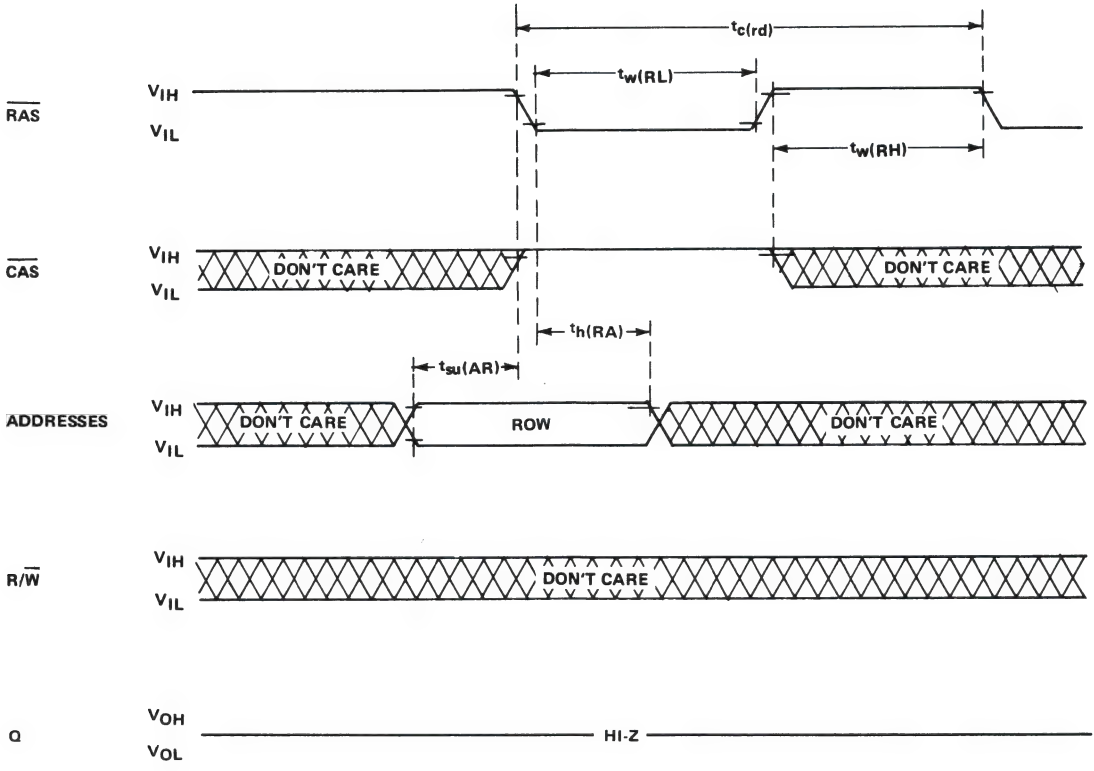
page-mode write cycle timing



*For Column Address:
A0 must be at V_{IL} for TMS 4108-0
A0 must be at V_{IH} for TMS 4108-1

$\overline{RAS}$-only refresh timing



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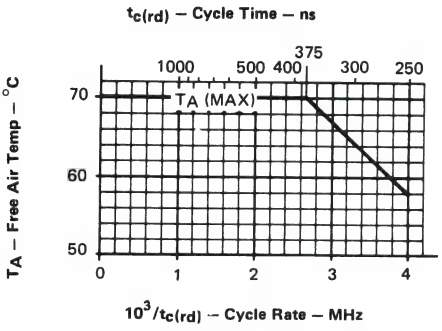
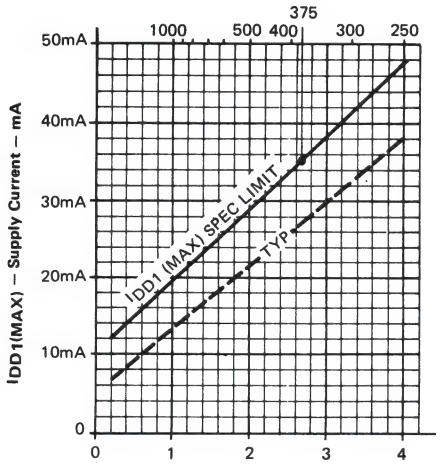
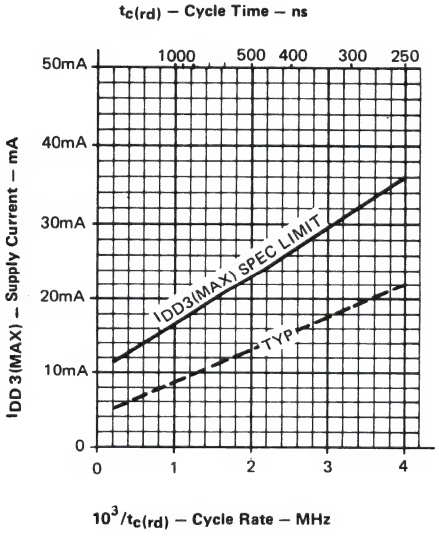
CYCLE RATE (& TIME) VS TEMPERATURE



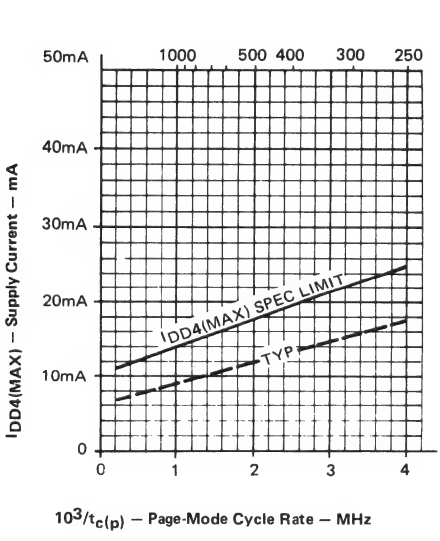
CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD1}



CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD3}



PAGE-MODE CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD4}



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TMS 4116 JDL, NL
16,384-BIT DYNAMIC RANDOM-ACCESS MEMORY

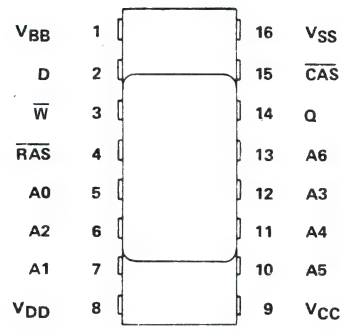
OCTOBER 1977

- 16,384 X 1 Organization
- 10% Tolerance on All Supplies
- All Inputs Including Clocks TTL-Compatible
- Unlatched Three-State Fully TTL-Compatible Output
- 3 Performance Ranges:

	ACCESS TIME ROW ADDRESS (MAX)	ACCESS TIME COLUMN ADDRESS (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY-WRITE† CYCLE (MIN)
TMS 4116-15	150 ns	100 ns	375 ns	375 ns
TMS 4116-20	200 ns	135 ns	375 ns	375 ns
TMS 4116-25	250 ns	165 ns	410 ns	515 ns

- Page-Mode Operation for Faster Access Time
- Common I/O Capability with "Early Write" Feature
- Low-Power Dissipation
  - Operating 462 mW (max)
  - Standby 20 mW (max)
- 1-T Cell Design, N-Channel Silicon-Gate Technology
- 16-Pin 300-Mil (7.62 mm) Package Configuration

16-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



PIN NOMENCLATURE			
A0-A6	Address Inputs	$\overline{W}$	Write Enable
$\overline{CAS}$	Column address strobe	V_{BB}	−5-V power supply
D	Data input	V_{CC}	+5-V power supply
Q	Data output	V_{DD}	+12-V power supply
$\overline{RAS}$	Row address strobe	V_{SS}	0 V ground

description

The TMS 4116 JL series is composed of monolithic high-speed dynamic 16,384-bit MOS random-access memories organized as 16,384 one-bit words, and employs single-transistor storage cells and N-channel silicon-gate technology.

All inputs and outputs are compatible with Series 74 TTL circuits including clocks: Row Address Strobe $\overline{RAS}$ (or $\overline{R}$) and Column Address Strobe $\overline{CAS}$ (or $\overline{C}$). All address lines (A0 through A6) and data-in (D) are latched on chip to simplify system design. Data out (Q) is unlatched to allow greater system flexibility.

Typical power dissipation is less than 350 milliwatts active and 6 milliwatts during standby (V_{CC} is not required during standby operation). To retain data, only 10 milliwatts average power is required which includes the power consumed to refresh the contents of the memory.

The TMS 4116 series is offered in 16-pin dual-in-line sidebraze (JDL suffix), and plastic (NL suffix) packages and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers.

operation

address (A0 through A6)

Fourteen address bits are required to decode 1 of 16,384 storage cell locations. Seven row-address bits are set up on pins A0 through A6 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the seven column-address bits are set up on pins A0 through A6 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

†The term "read-write cycle" is sometimes used as an alternative title to "read-modify-write cycle".

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write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. The latter falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the enable time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every two milliseconds to retain data. Since the output buffer is in the high-impedance state unless $\overline{CAS}$ is applied, the $\overline{RAS}$ only refresh sequence avoids any output during refresh. Strobing each of the 128 row addresses (A0 through A6) with $\overline{RAS}$ causes all bits in each row to be refreshed. $\overline{CAS}$ remains high (inactive) for this refresh sequence, thus conserving power.

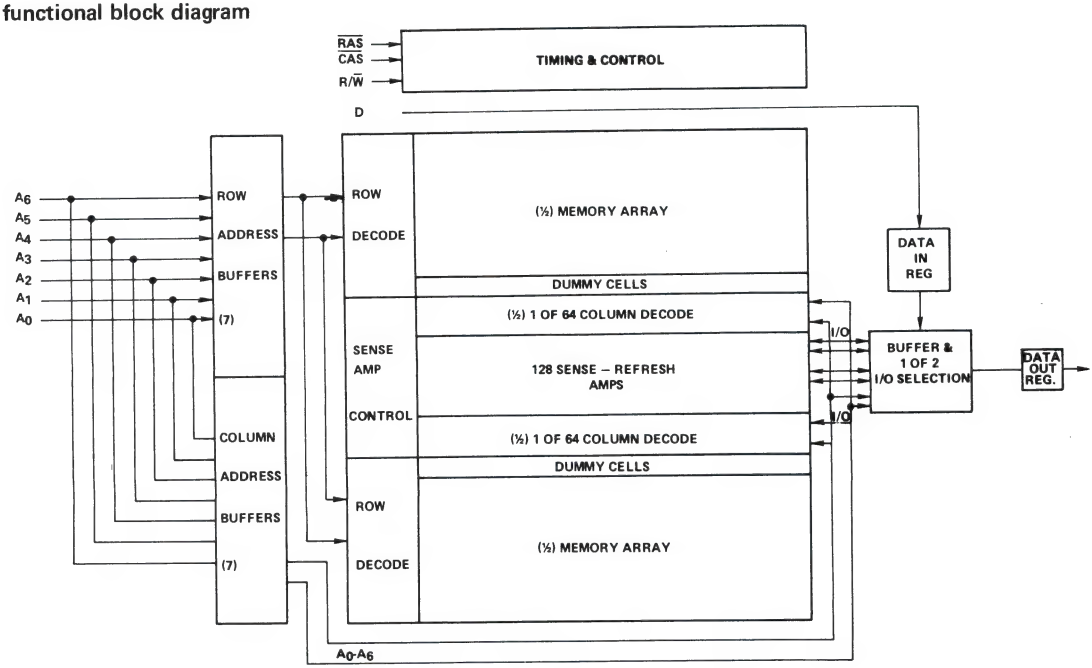
page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses on the same page is eliminated. To extend beyond the 128 column locations on a single RAM, the row address and $\overline{RAS}$ is applied to multiple 16K RAMs $\overline{CAS}$ is decoded to select the proper RAM.

power-up

V_{BB} must be applied to the device either before or at the same time as the other supplies and removed last. Failure to observe this precaution will cause dissipation in excess of the absolute maximum ratings due to internal forward bias conditions. This also applies to system use, where failure of the V_{BB} supply must immediately shut down the other supplies. After power up, eight memory cycles must be performed to achieve proper device operation.

functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin (see Note 1)	−0.5 to 20 V
Voltage on V_{CC}, V_{DD} supplies with respect to V_{SS}	−1 to 15 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}		−4.5	−5	−5.5	V
Supply voltage, V_{CC}		4.5	5	5.5	V
Supply voltage, V_{DD}		10.8	12	13.2	V
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}	All inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.4		7	V
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	2.7		7	
Low-level input voltage, V_{IL}		−1	0	0.8	V
Refresh time, $t_{refresh}$				2	ms
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
I_I	Input current (leakage)	V_I = 0 V to 7 V, All other pins = 0 V except V_{BB} = −5 V	−10		10	μA
I_O	Output current (leakage)	V_O = 0 to 5.5 V, $\overline{CAS}$ high	−10		10	μA
I_{BB1}	Average operating current	Minimum cycle time		50	200	μA
I_{CC1}*	during read or write				4**	mA
I_{DD1}	cycle			27	35	mA
I_{BB2}	Standby current	After 1 memory cycle		10	100	μA
I_{CC2}		$\overline{RAS}$ and $\overline{CAS}$	−10		10	μA
I_{DD2}		high		0.5	1.5	mA
I_{BB3}	Average refresh current	Minimum cycle time		50	200	μA
I_{CC3}		$\overline{RAS}$ cycling,	−10		10	μA
I_{DD3}		$\overline{CAS}$ high		20	27	mA
I_{BB4}	Average page-mode	Minimum cycle time		50	200	μA
I_{CC4}*	current	$\overline{RAS}$ low,			4**	
I_{DD4}		$\overline{CAS}$ cycling		20	27	mA

*V_{CC} is applied only to the output buffer, so I_{CC} depends on output loading.
**Output loading two standard TTL loads.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	5	pF
$C_{i(D)}$	Input capacitance, data input	4	5	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	10	pF
$C_{i(W)}$	Input capacitance, write enable input	8	10	pF
C_o	Output capacitance	5	7	pF

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS 4116-15		TMS 4116-20		TMS 4116-25		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135		165	ns
$t_{a(R)}$	Access time from row address strobe	t_{RLCL} = MAX, C_L = 100 pF Load = 2 Series 74 TTL gates	t_{RAC}		150		200		250	ns
t_{PXZ}	Output disable time	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	0	60	ns

†All typical values are at T_A = 25°C and nominal supply voltages.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS 4116-15		TMS 4116-20		TMS 4116-25		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	170		225		275		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	375		375		410		ns
$t_{c(W)}$	Write cycle time	t_{WC}	375		375		410		ns
$t_{c(RW)}$	Read, modify-write cycle time	t_{RWC}	375		375		515		ns
$t_{w(CH)}$	Pulse width, column address strobe high (precharge time)	t_{CP}	60		80		100		ns
$t_{w(CL)}$	Pulse width, column address strobe low	t_{CAS}	100	10,000	135	10,000	165	10,000	ns
$t_{w(RH)}$	Pulse width, row address strobe high (precharge time)	t_{RP}	100		120		150		ns
$t_{w(RL)}$	Pulse width, row address strobe low	t_{RAS}	150	10,000	200	10,000	250	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		75		ns
t_T	Transition times (rise and fall) for $\overline{RAS}$ and $\overline{CAS}$	t_T	3	35	3	50	3	50	ns
$t_{su(AC)}$	Column address setup time	t_{ASC}	−10		−10		−10		ns
$t_{su(AR)}$	Row address setup time	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		0		ns
$t_{su(WCH)}$	Write command setup time before $\overline{CAS}$ high	t_{CWL}	60		80		100		ns
$t_{su(WRH)}$	Write command setup time before $\overline{RAS}$ high	t_{RWL}	60		80		100		ns
$t_{h(ACL)}$	Column address hold time after $\overline{CAS}$ low	t_{CAH}	45		55		75		ns
$t_{h(AR)}$	Row address hold time	t_{RAH}	20		25		35		ns
$t_{h(ARL)}$	Column address hold time after $\overline{RAS}$ low	t_{AR}	95		120		160		ns
$t_{h(CRL)}$	$\overline{CAS}$ hold time after $\overline{RAS}$ low	t_{CSH}	150		200		250		ns
$t_{h(DCL)}$	Data hold time after $\overline{CAS}$ low	t_{DH}	45		55		75		ns
$t_{h(DRL)}$	Data hold time after $\overline{RAS}$ low	t_{DHR}	95		120		160		ns
$t_{h(DWL)}$	Data hold time after $\overline{W}$ low	t_{DH}	45		55		75		ns
$t_{h(rd)}$	Read command hold time	t_{RCH}	0		0		0		ns
$t_{h(WCL)}$	Write command hold time after $\overline{CAS}$ low	t_{WCH}	45		55		75		ns
$t_{h(WRL)}$	Write command hold time after $\overline{RAS}$ low	t_{WCR}	95		120		160		ns
t_{CHRL}	Delay time, column address strobe high to row address strobe	t_{CRP}	−20		−20		−20		ns
t_{CLRH}	Delay time, column address strobe low to row address strobe high	t_{RSH}	100		135		165		ns
t_{CLWL}	Delay time, column address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{CWD}	70		95		125		ns
t_{REF}	Refresh period	t_{REF}		2		2		2	ms
t_{RLCL}	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	35	85	ns
t_{RLWL}	Delay time, row address strobe low to $\overline{W}$ low (read, modify-write cycle only)	t_{RWD}	120		160		200		ns
t_{WLCL}	Delay time, $\overline{W}$ low to column address strobe low (early write cycle)	t_{WCS}	−20		−20		−20		ns

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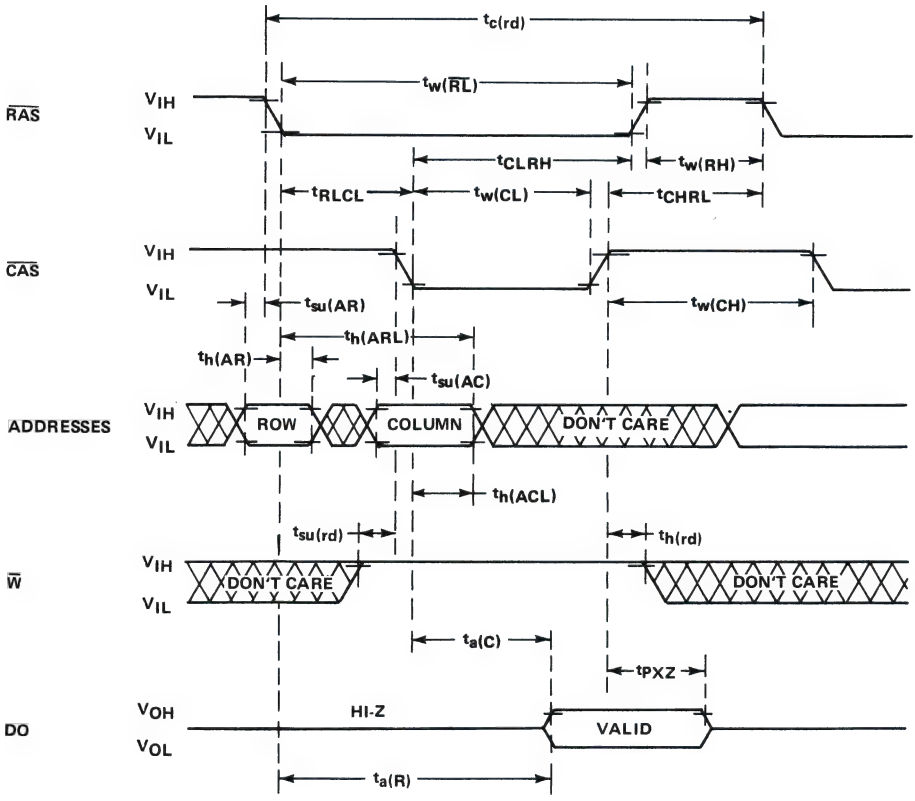
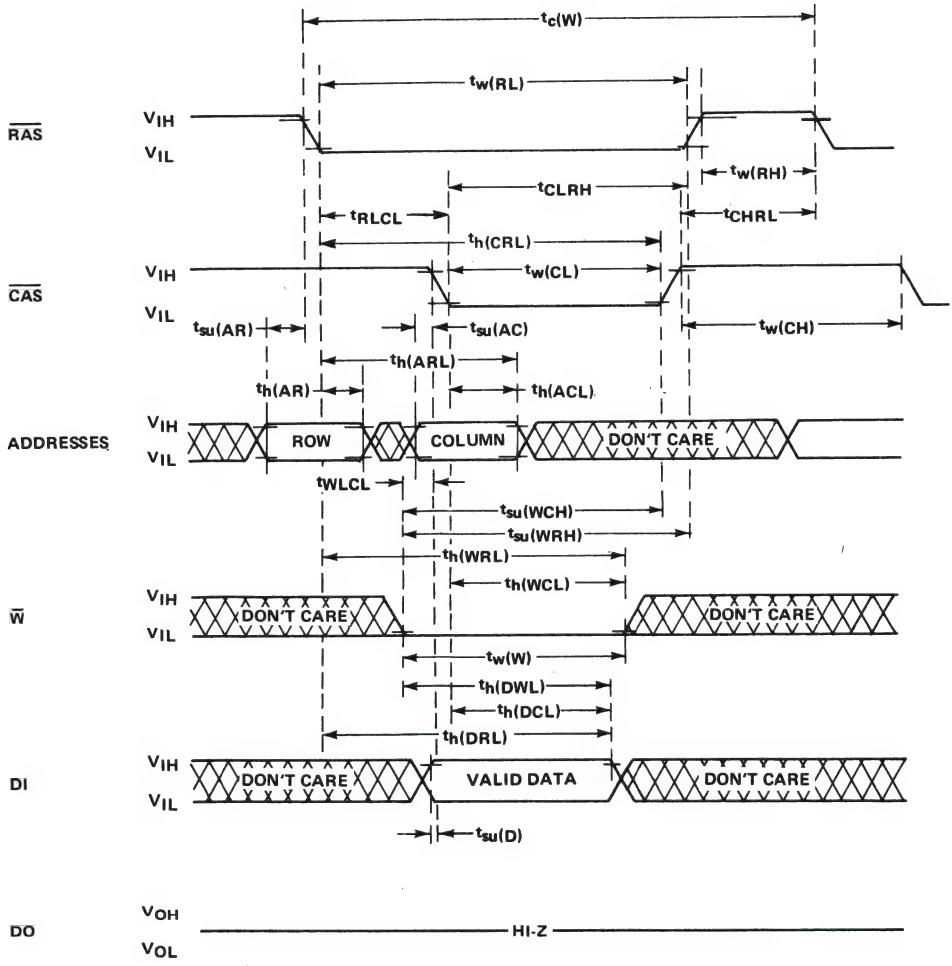
read cycle timing



early write cycle timing



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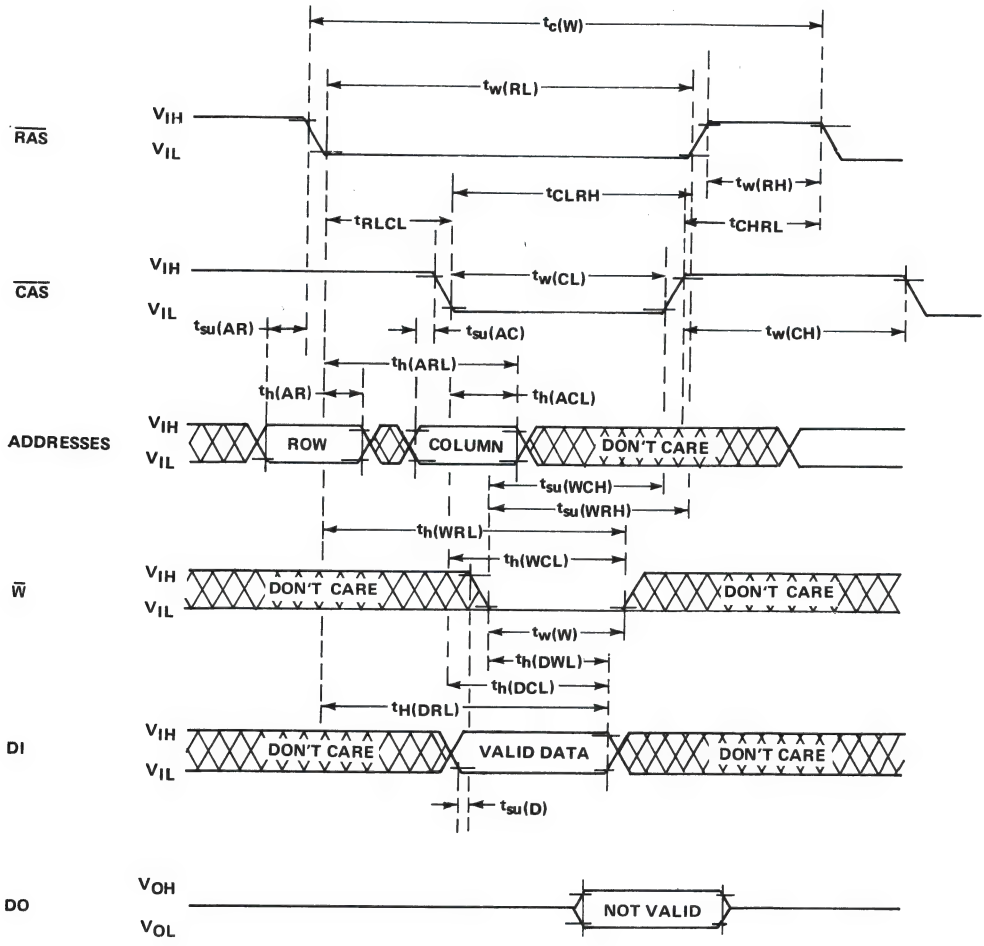
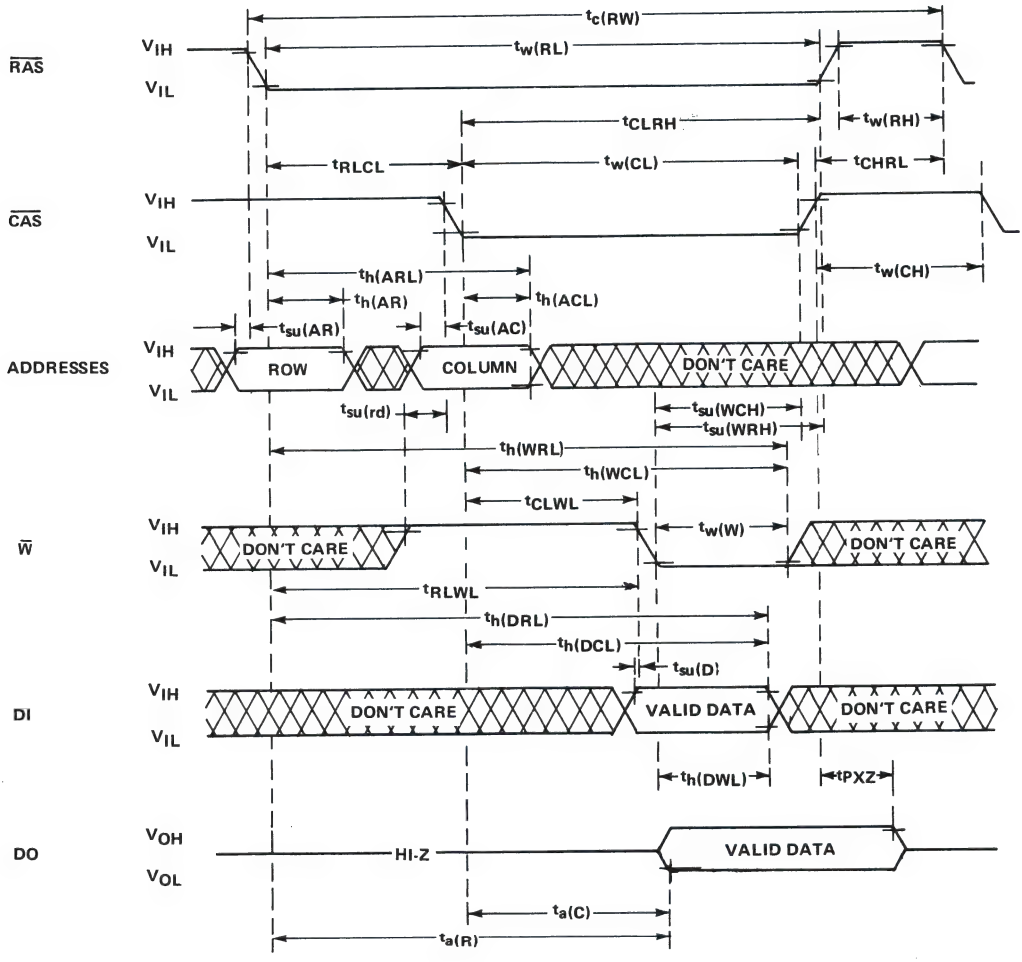
write cycle timing



read-write/read-modify-write cycle timing



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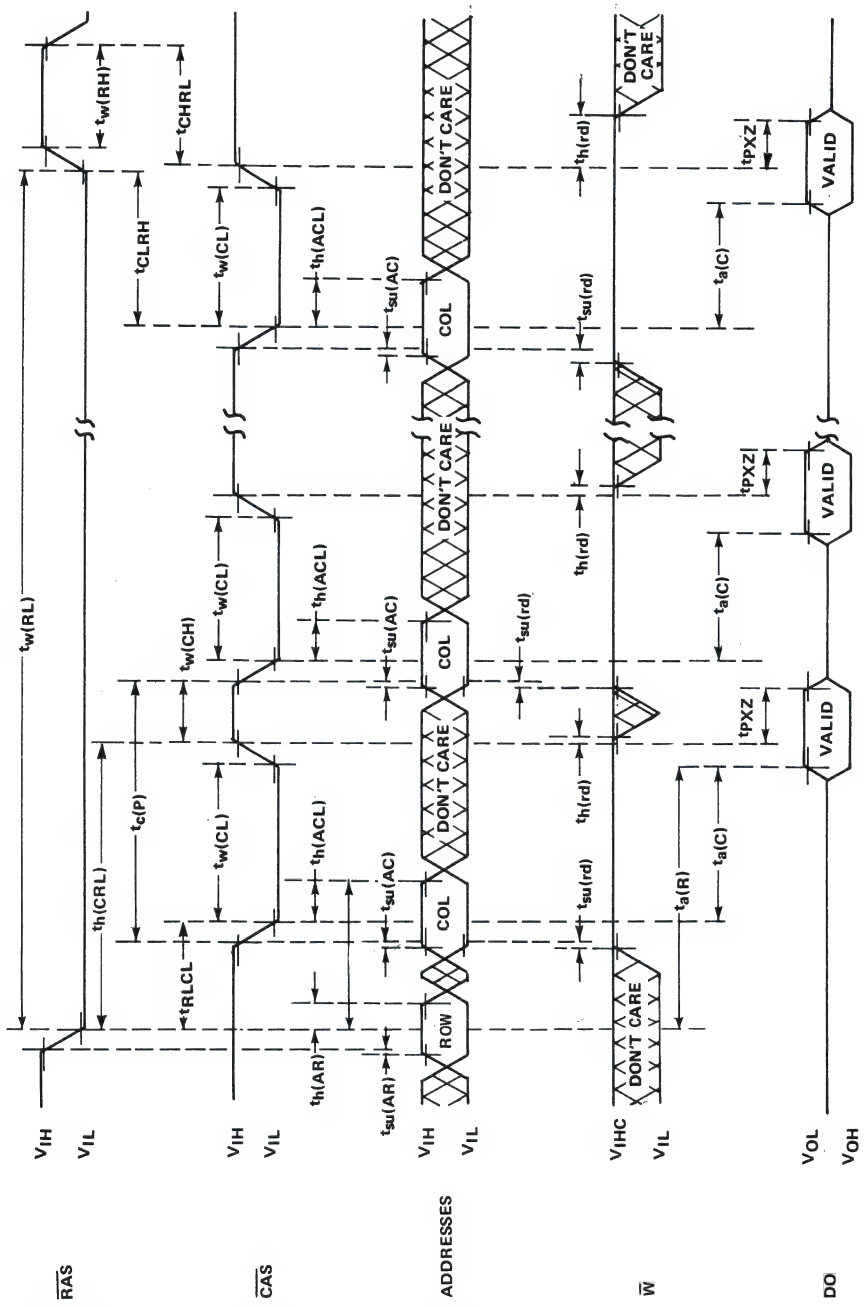
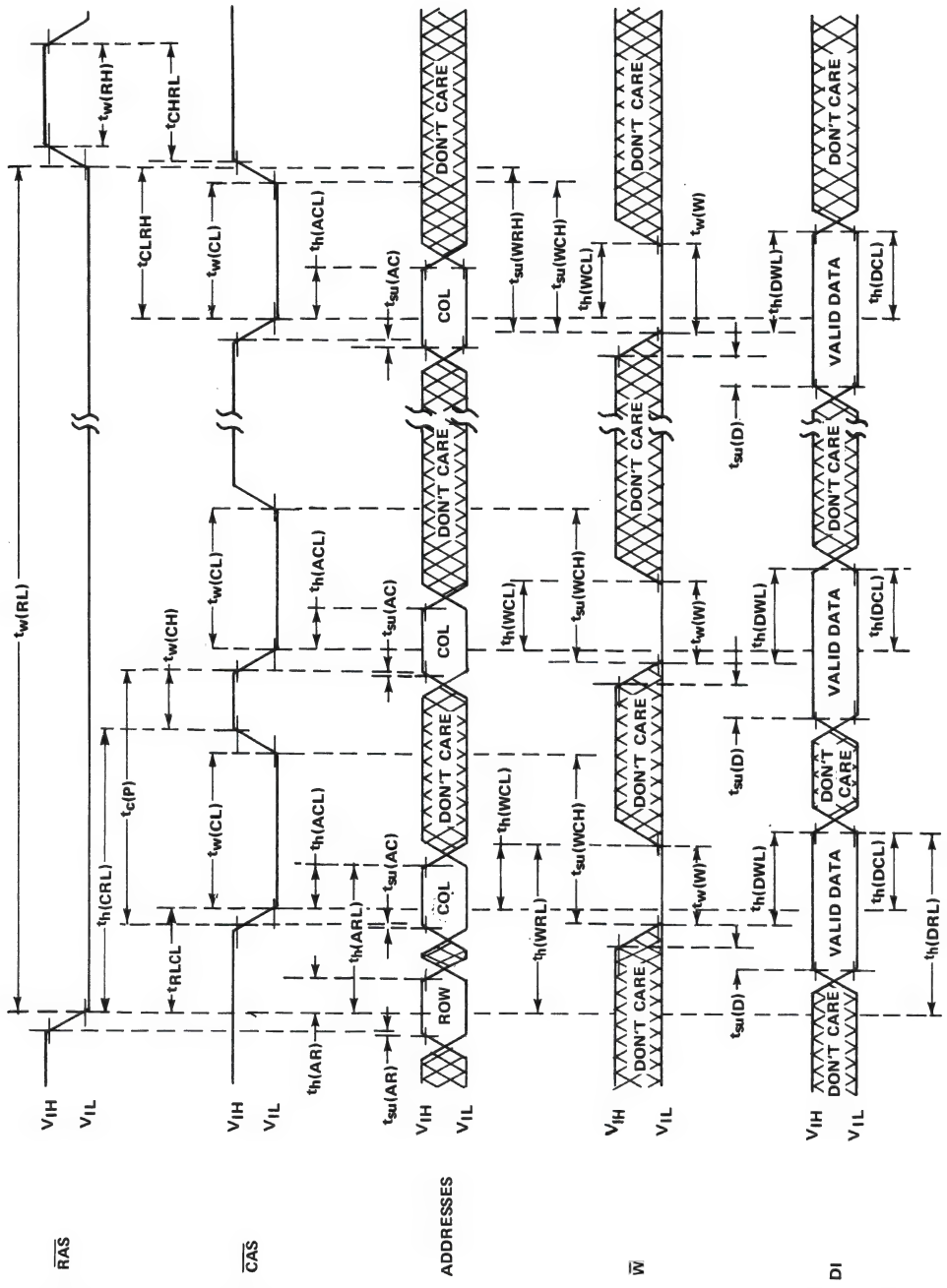
page-mode read cycle timing



page-mode write cycle timing



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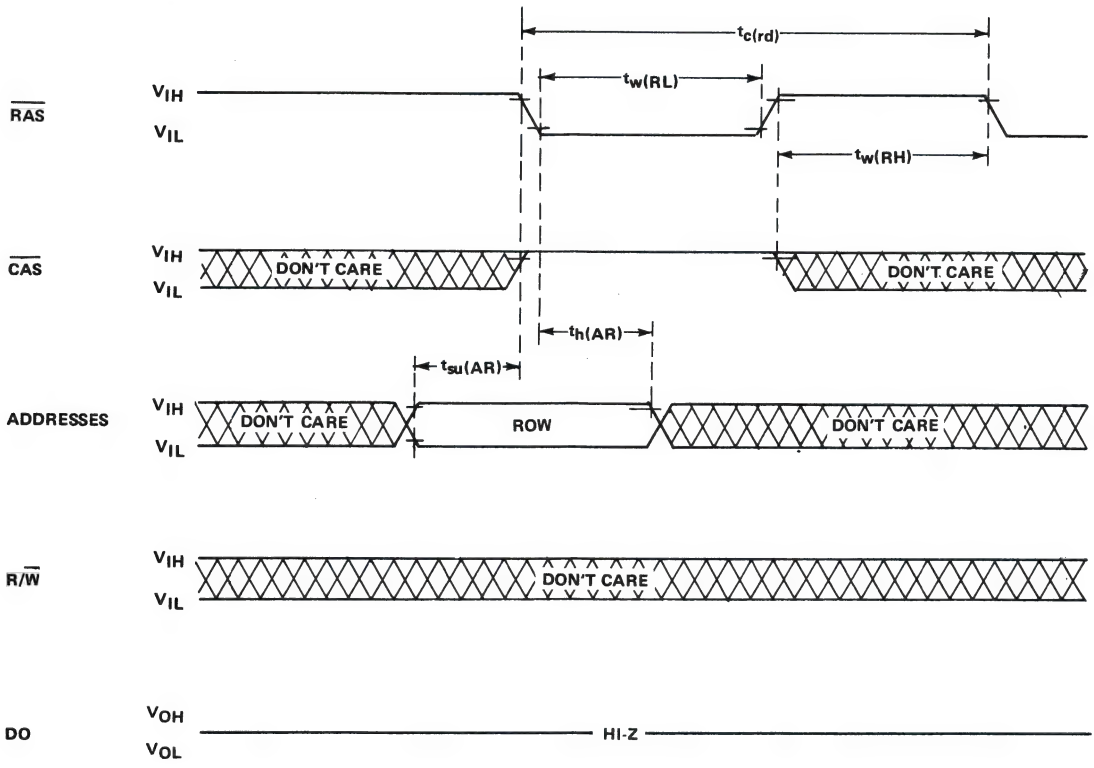
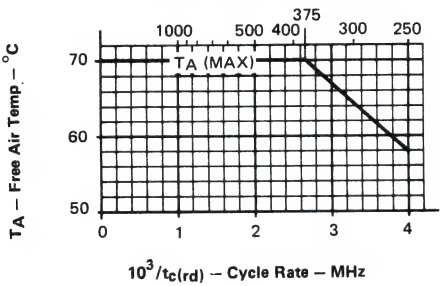
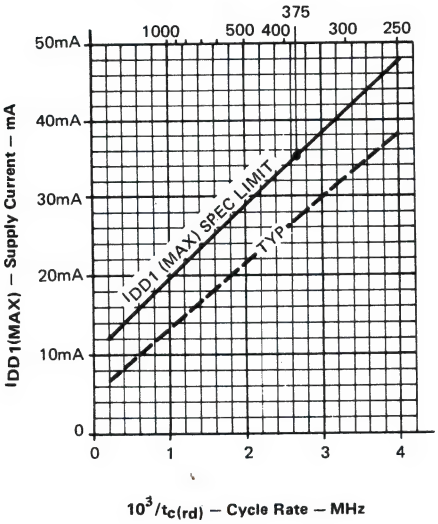
$\overline{\text{RAS}}$-only refresh timing



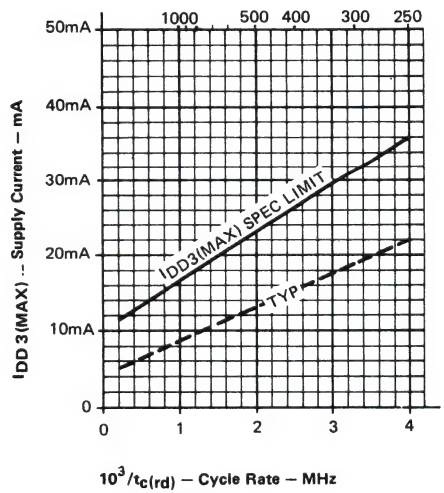
CYCLE RATE (& TIME) VS TEMPERATURE



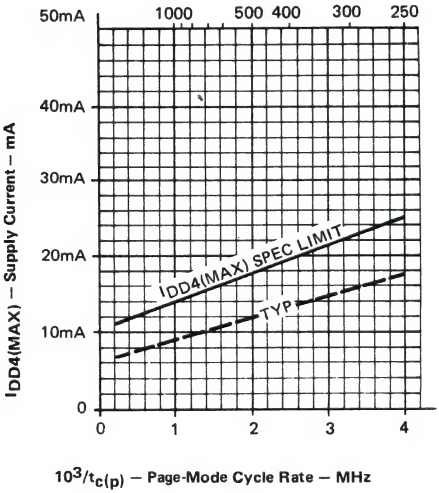
CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD1}



CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD3}



PAGE-MODE CYCLE RATE (& TIME) vs MAX SUPPLY CURRENT, I_{DD4}



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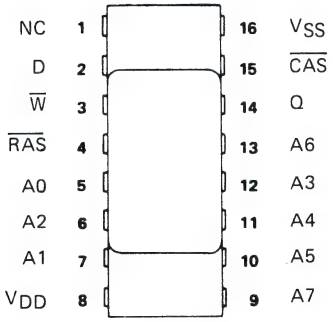
TMS 4164 JDL
65,536-BIT DYNAMIC RANDOM-ACCESS MEMORY

DECEMBER 1979

- 65,536 X 1 Organization
- Single +5 V Supply (10% Tolerance)
- JEDEC Standardized Pin Out
- Upward Pin Compatible with TMS 4116 (16K Dynamic RAM)
- Max Access Time from RAS less than 150 ns
- Min Cycle time (Read or Write) less than 260 ns
- Long Refresh Period . . . 4 milliseconds
- Low Refresh Overhead Time . . . As Low As 1.6% of Total Refresh Period
- All Inputs, Outputs, Clocks Fully TTL Compatible
- 3-State Unlatched Outputs
- Common I/O Capability with "Early Write" Feature
- Page-mode Operation for Faster Access
- Low Power Dissipation
  — Operating . . . 125 mW (typ.)
  — Standby . . . 17.5 mW (typ.)
- New SMOS (Scaled-MOS) N-Channel Technology

16-PIN CERAMIC DUAL-IN-LINE PACKAGE (TOP VIEW)



PIN NOMENCLATURE	
A0-A7	Address Inputs
CAS	Column Address Strobe
D	Data In
NC	No-Connect
Q	Data Out
RAS	Row Address Strobe
W	Write Enable
V_{DD}	+5 V Supply
V_{SS}	Ground

description

The TMS 4164 JDL is a high speed 65,536 bit dynamic random access memory organized as 65,536 words of one bit each. It employs state-of-the-art SMOS (scaled MOS) N-channel double level polysilicon gate technology for very high performance combined with low cost and improved reliability.

The TMS 4164 JDL features RAS access times to 150 ns maximum. Power dissipation is 125 mW typical operating, 17.5 mW typical standby.

New SMOS technology permits operation from single +5 V supply, reducing system power supply and decoupling requirements, and easing board layout. I_{DD} peaks have been reduced to 60 mA typical, and a −1 V input voltage undershoot can be tolerated, minimizing system noise considerations.

Refresh period is extended to 4 milliseconds, and during this period each of the 256 rows must be strobed with RAS in order to retain data. CAS can remain high during the refresh sequence to conserve power.

All inputs and outputs, including clocks, are compatible with Series 74 TTL. All address lines and data-in are latched on chip to simplify system design. Data-out is unlatched to allow greater system flexibility. Pin 1 is no connect to allow compatibility with other 64K RAMs using this pin for an additional function.

The TMS 4164 JDL is offered in a 16 pin dual-in-line ceramic sidebraze package and is guaranteed for operation from 0°C to 70°C. Packages are designed for insertion in mounting-hole rows on 300 mil (7.62 mm) centers.

operation

address (A0 through A7)

Sixteen address bits are required to decode 1 of 65,536 storage cell locations. Eight row-address bits are set up on pins A0 through A7 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then the eight column-address bits are set up on pins A0 through A7 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select activating the column decoder and the input and output buffers.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$, data-out will remain in the high-impedance state for the entire cycle permitting common I/O operation.

data-in (D)

Data is written during a write or read-modify write cycle. The falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. This latch can be driven from standard TTL circuits without a pull-up resistor. In an early write cycle $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal.

data-out (Q)

The three state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fan-out of two Series 74 TTL loads. Data-out is the same polarity as data-in. The output is in the high-impedance (floating) state until $\overline{CAS}$ is brought low. In a read cycle the output goes active after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ is satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ is low; $\overline{CAS}$ going high returns it to a high-impedance state. In an early write cycle, the output is always in the high-impedance state. In a delayed write or read-modify-write cycle, the output will follow the sequence for the read cycle.

refresh

A refresh operation must be performed at least every four milliseconds to retain data. Since the output buffer is in the high-impedance state unless CAS is applied, the RAS only refresh sequence avoids any output during refresh. Strobing each of the 256 row addresses (A0 through A7) with RAS causes all bits in each row to be refreshed. CAS can remain high (inactive) for this refresh sequence to conserve power.

page mode

Page mode operation allows effectively faster memory access by keeping the same row address and strobing successive column addresses onto the chip. Thus, the time required to setup and strobe sequential row addresses for the same page is eliminated. To extend beyond the 256 column locations on a single RAM, the row address and $\overline{RAS}$ are applied to multiple 64K RAMs. $\overline{CAS}$ is then decoded to select the proper RAM.

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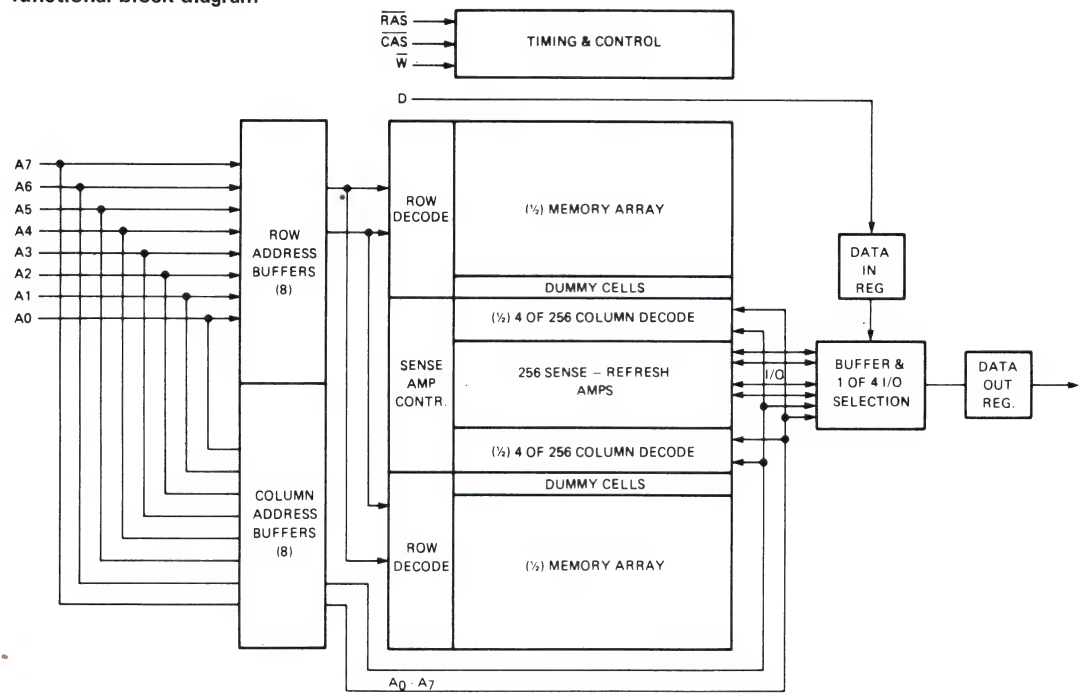
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Voltage on any pin except V_{DD} and data out (see Note 1) . . . . . –1.5 to 10 V
Voltage on V_{DD} supply and data out with respect to V_{SS} . . . . . –1 to 6 V
Short circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.4		V_{DD}+0.3	V
Low-level input voltage, V_{IL}	–1		0.8	V
Refresh time, $t_{refresh}$			4	ms
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
*	V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4			V
*	V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA			0.4	V
	I_I	Input current (leakage)	V_I = 0 V to 5.8 V, All other pins = 0 V	−10		10	μA
	I_O	Output current (leakage)	V_O = 0.4 to 5.5 V, CAS high	−10		10	μA
	I_{DD1}	Average operating current during read or write cycle	Minimum cycle time		25	37	mA
	I_{DD2}	Standby current	After 1 memory cycle, RAS and CAS high		3.5	5	mA
	I_{DD3}	Average refresh current	Minimum cycle time, RAS cycling, CAS high		20	32	mA
	I_{DD4}	Average page-mode current	Minimum cycle time, RAS low, CAS cycling		20	32	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	UNIT
$C_{i(A)}$	Input capacitance, address inputs	4	pF
$C_{i(D)}$	Input capacitance, data input	4	pF
$C_{i(RC)}$	Input capacitance, strobe inputs	8	pF
$C_{i(W)}$	Input capacitance, write enable input	8	pF
C_o	Output capacitance	5	pF

† All typical values are at T_A = 25°C and nominal supply voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	ALT. SYMBOL	TMS 4164-15		TMS 4164-20		UNIT
				MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from column address strobe	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{CAC}		100		135	ns
$t_{a(R)}$	Access time from row address strobe	t_{RLCL} = MAX, C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{RAC}		150		200	ns
t_{PXZ}	Output disable time	C_L = 100 pF, Load = 2 Series 74 TTL gates	t_{OFF}	0	40	0	50	ns

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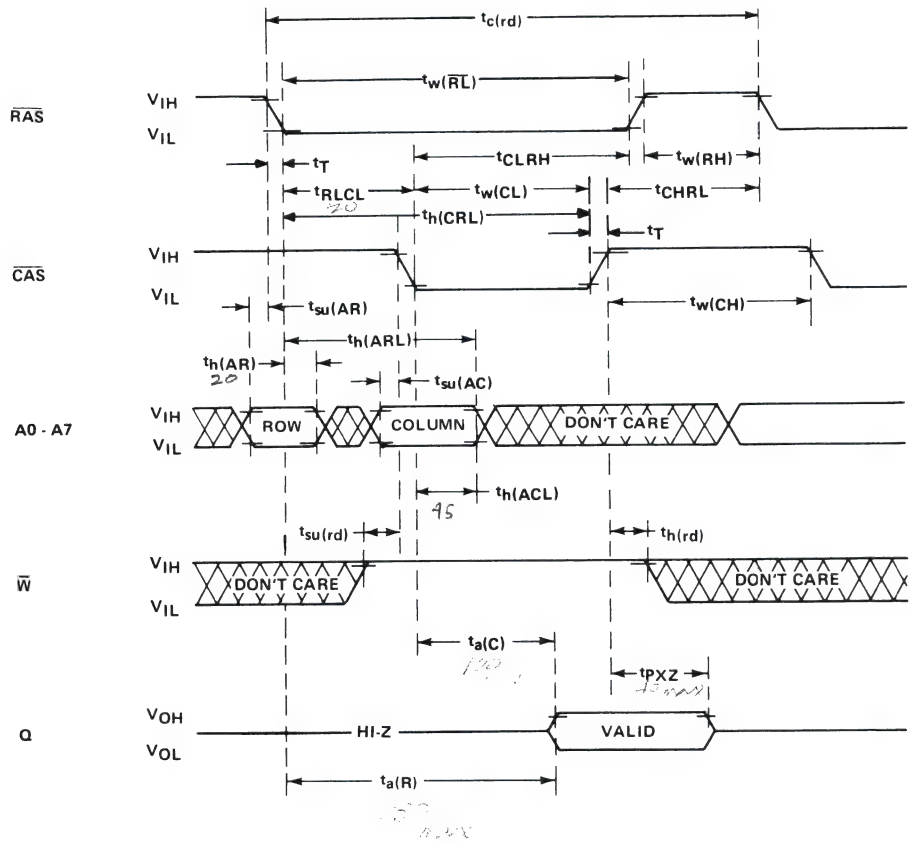
timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		ALT. SYMBOL	TMS 4164-15		TMS 4164-20		UNIT
			MIN	MAX	MIN	MAX	
$t_{c(P)}$	Page mode cycle time	t_{PC}	156		206		ns
$t_{c(rd)}$	Read cycle time	t_{RC}	256		326		ns
$t_{c(W)}$	Write cycle time	t_{WC}	256		326		ns
$t_{c(RW)}$	Read-write/read-modify-write cycle time	t_{RWC}	256		326		ns
$t_{w(CH)}$	Pulse width, column address strobe high (precharge time)*	t_{CP}	50		80		ns
$t_{w(CL)}$	Pulse width, column address strobe low	t_{CAS}	100	10,000	135	10,000	ns
$t_{w(RH)}$	Pulse width, row address strobe high (precharge time)	t_{RP}	100		120		ns
$t_{w(RL)}$	Pulse width, row address strobe low	t_{RAS}	150	10,000	200	10,000	ns
$t_{w(W)}$	Write pulse width	t_{WP}	45		55		ns
t_T	Transition times (rise and fall) for RAS and CAS	t_T	3	35	3	35	ns
$t_{su(AC)}$	Column address setup time	t_{ASC}	−5		−5		ns
$t_{su(AR)}$	Row address setup time	t_{ASR}	0		0		ns
$t_{su(D)}$	Data setup time	t_{DS}	0		0		ns
$t_{su(rd)}$	Read command setup time	t_{RCS}	0		0		ns
$t_{su(WCH)}$	Write command setup time before CAS high	t_{CWL}	60		80		ns
$t_{su(WRH)}$	Write command setup time before RAS high	t_{RWL}	60		80		ns
$t_{h(ACL)}$	Column address hold time after CAS low	t_{CAH}	45		55		ns
$t_{h(AR)}$	Row address hold time	t_{RAH}	20		25		ns
$t_{h(ARL)}$	Column address hold time after RAS low	t_{AR}	95		120		ns
$t_{h(CRL)}$	CAS hold time after RAS low	t_{CSH}	150		200		ns
$t_{h(DCL)}$	Data hold time after CAS low	t_{DH}	45		55		ns
$t_{h(DRL)}$	Data hold time after RAS low	t_{DHR}	95		120		ns
$t_{h(DWL)}$	Data hold time after W low	t_{DH}	45		55		ns
$t_{h(rd)}$	Read command hold time	t_{RCH}	0		0		ns
$t_{h(WCL)}$	Write command hold time after CAS low	t_{WCH}	45		55		ns
$t_{h(WRL)}$	Write command hold time after RAS low	t_{WCR}	95		120		ns
t_{CHRL}	Delay time, column address strobe high to row address strobe low	t_{CRP}	0		0		ns
t_{CLRH}	Delay time, column address strobe low to row address strobe high	t_{RSH}	100		135		ns
t_{CLWL}	Delay time, column address strobe low to W low (read, modify-write-cycle only)	t_{CWD}	40		50		ns
t_{RLCL}	Delay time, row address strobe low to column address strobe low (maximum value specified only to guarantee access time)	t_{RCD}	20	50	25	65	ns
t_{RLWL}	Delay time, row address strobe low to W low (read, modify-write-cycle only)	t_{RWD}	90		100		ns
t_{WLCL}	Delay time, W low to column address strobe low (early write cycle)	t_{WCS}	−5		−5		ns

* Page Mode Only

read cycle timing



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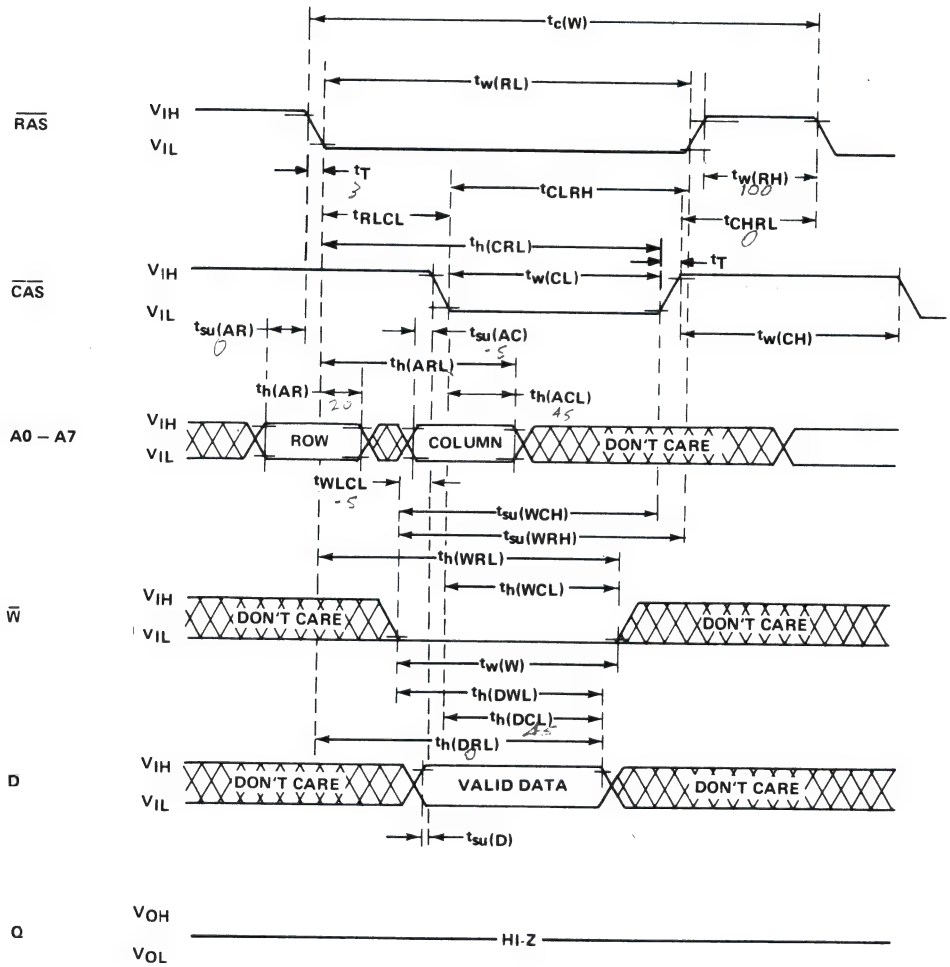
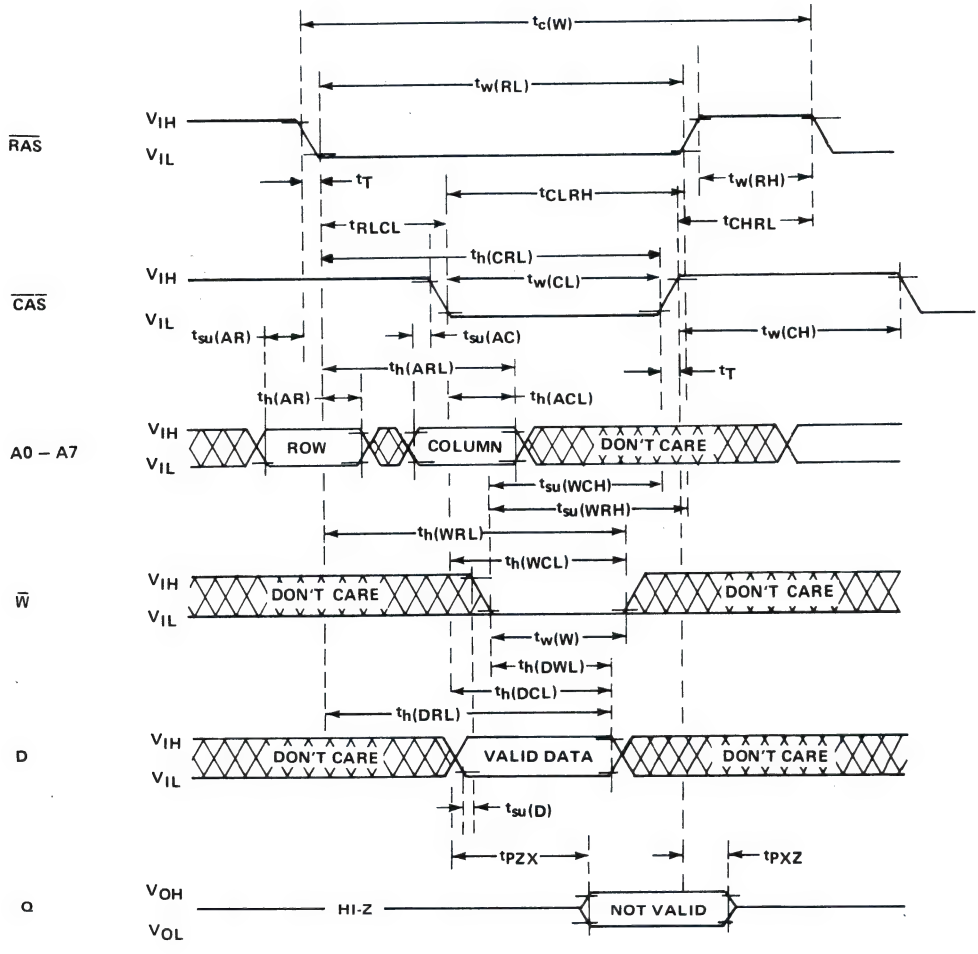
early write cycle timing



write cycle timing



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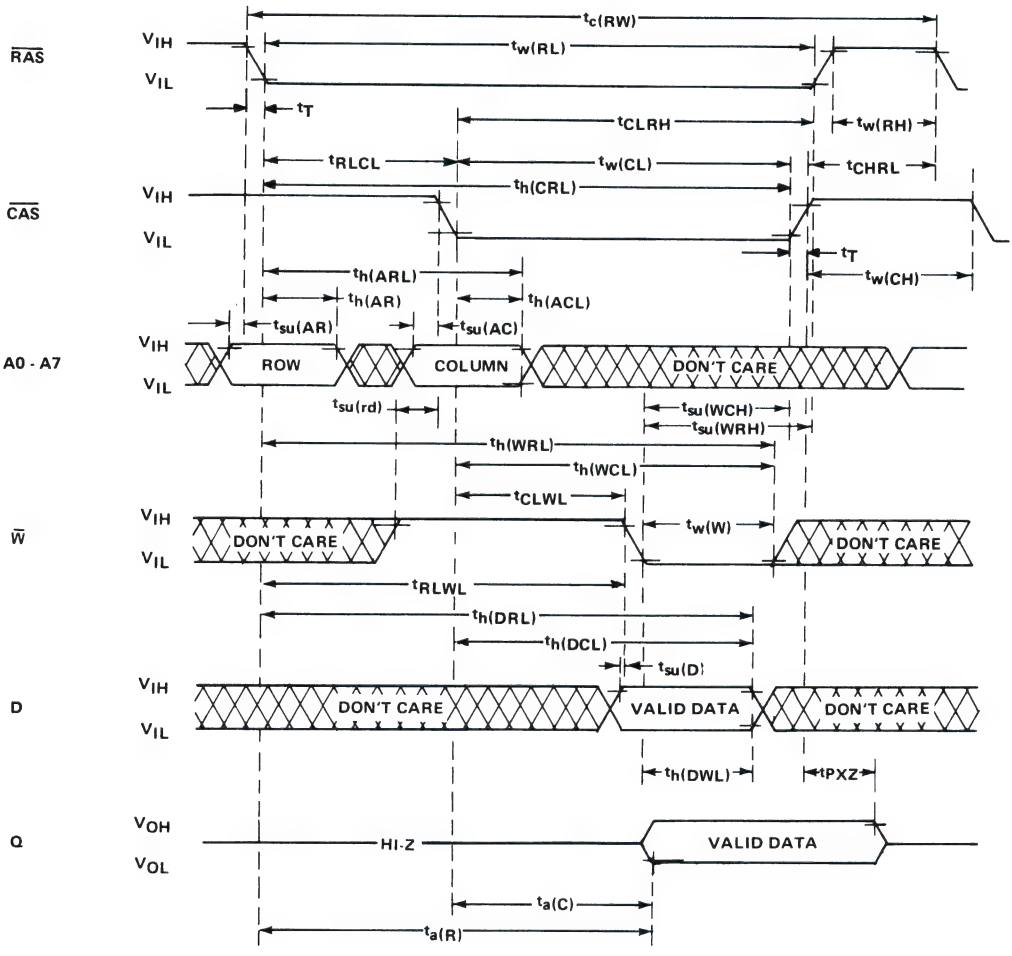
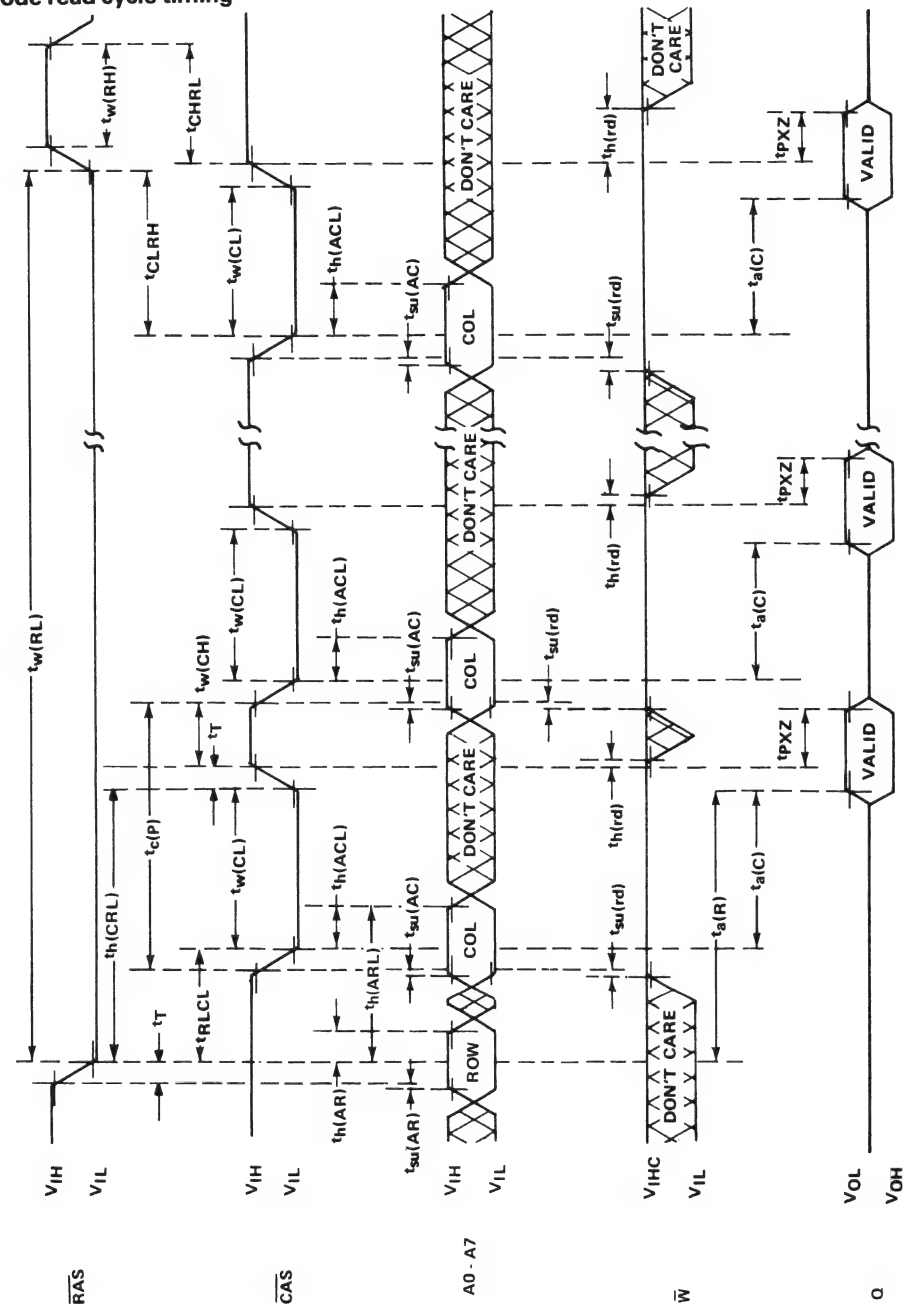
read-write/read-modify-write cycle timing



page-mode read cycle timing



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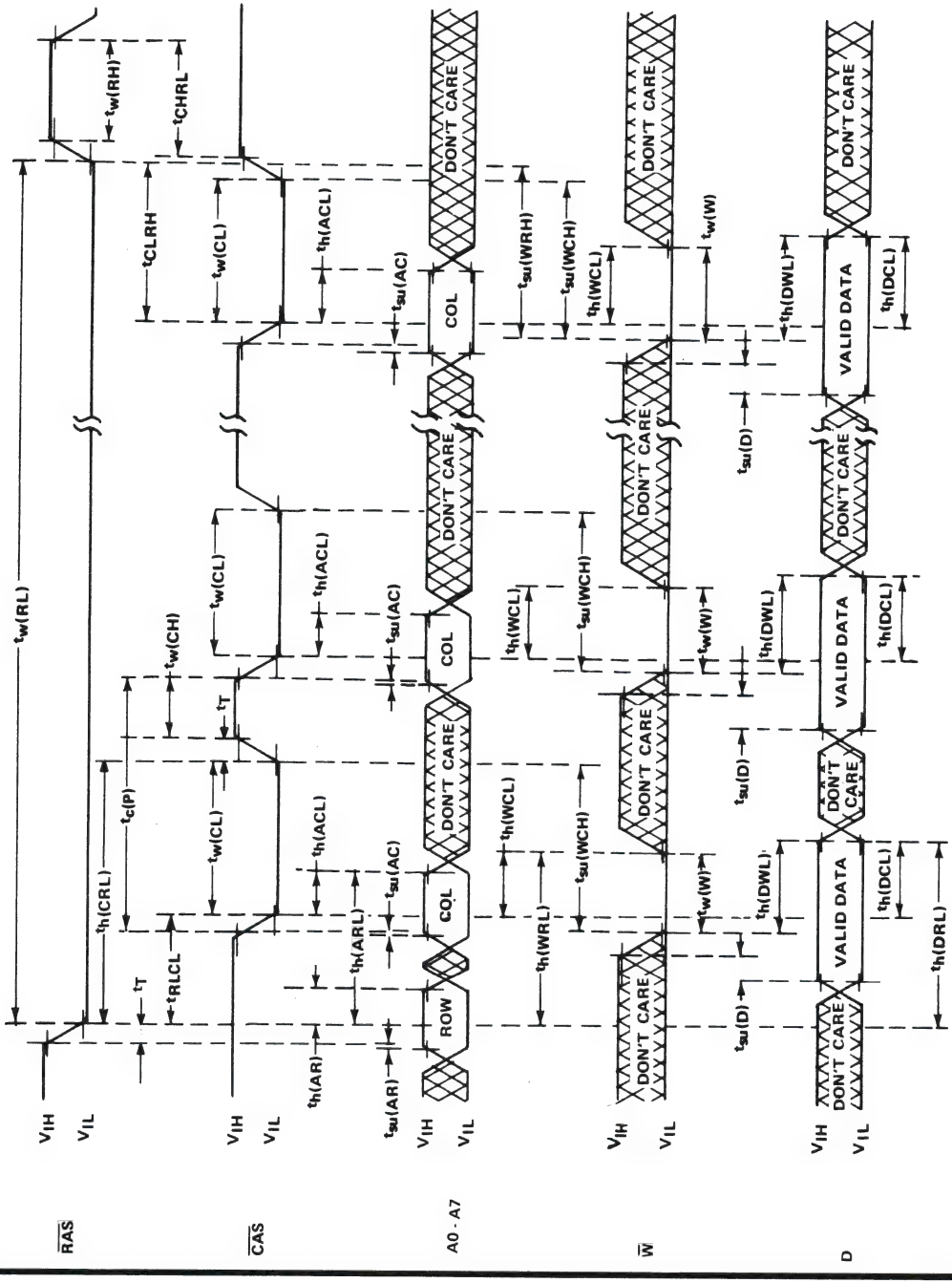
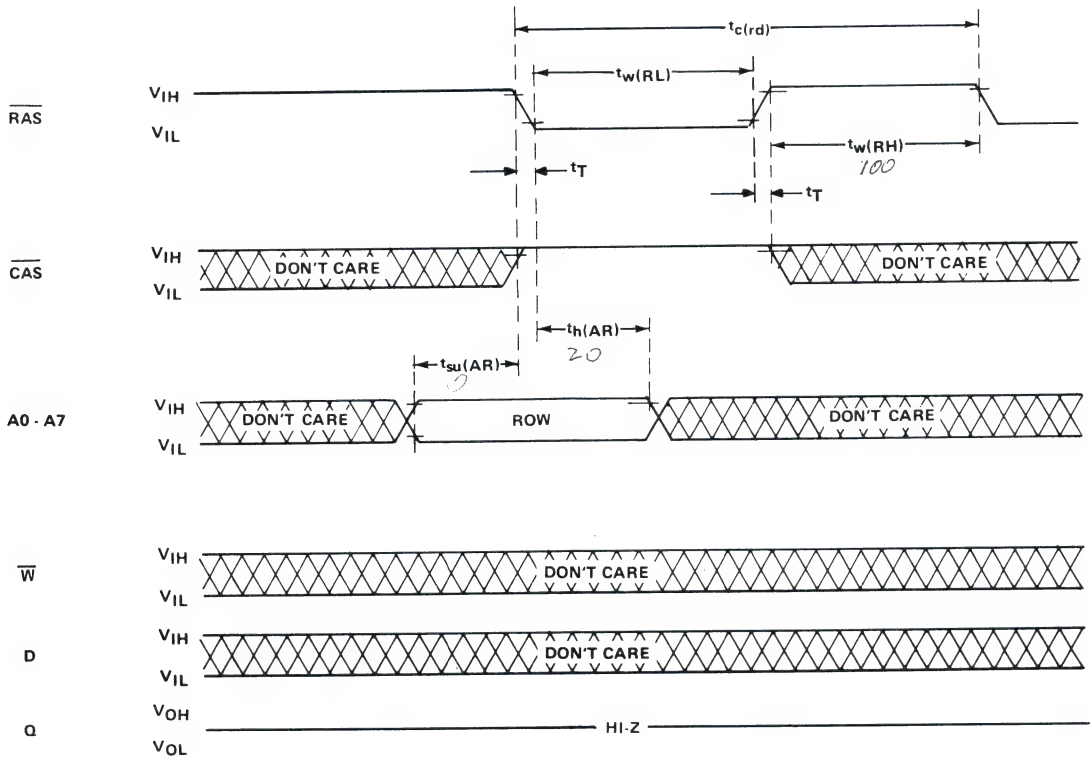
page-mode write cycle timing



$\overline{RAS}$-only refresh timing



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STATIC RAM DATA SHEETS

TMS 4044 NL; TMS 40L44 NL
4096-WORD BY 1-BIT STATIC RAMS

DECEMBER 1979

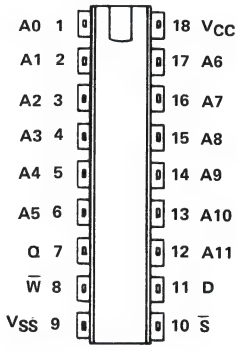
- Single +5 V Supply (±10% Tolerance)
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)
TMS 4044-15, TMS 40L44-15	150 ns	150 ns
TMS 4044-20, TMS 40L44-20	200 ns	200 ns
TMS 4044-25, TMS 40L44-25	250 ns	250 ns
TMS 4044-45, TMS 40L44-45	450 ns	450 ns

- 400-mV Guranteed DC Noise Immunity with Standard TTL Loads — No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)	MAX (STANDBY)
TMS 4044	440 mW	156 mW
TMS 40L44	275 mW	96 mW

TMS 4044/TMS 40L44
18-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NAMES

A0-A11	Addresses
D	Data In
Q	Data Out
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. All versions are characterized to retain data at V_{CC} = 2.4 V to reduce power dissipation.

The TMS 4044/40L44 series is offered in the 18-pin dual-in-line plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.
for operation from 0°C to 70°C.

operation

addresses (A0-A11)

The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in (D)

Data can be written into a selected device when the write enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

data-out (Q)

The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The output is in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

standby operation

The standby mode, which will retain data while reducing power consumption, is attained by recuding the V_{CC} supply from 5 volts to 2.4 volts. When reducing supply voltage during the standby mode, $\overline{S}$ and $\overline{W}$ must be high to retain data. The V_{CC} transition rate should not exceed 26 mV/ms. During standby operation, data can not be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady state operating conditions.

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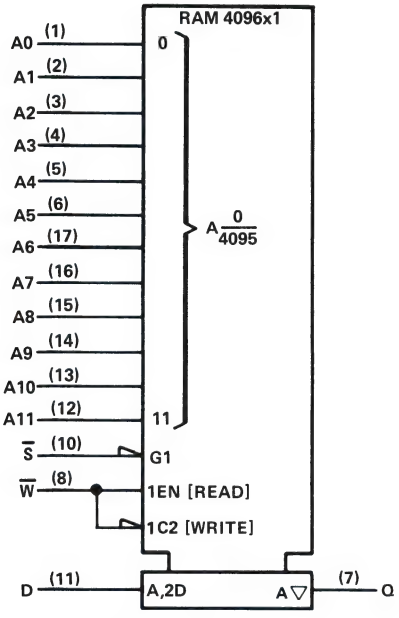
absolute maximum ratings over operating free-air temperature (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . –1 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

FUNCTION TABLE

INPUTS		OUTPUT	MODE
$\overline{S}$	$\overline{W}$	Q	
H	X	HI-Z	NOT SELECTED
L	L	HI-Z	WRITE
L	H	DATA OUT	READ

recommended operating conditions

PARAMETER		TMS 4044-45 TMS 40L44-45			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC}	Operating	4.5	5	5.5	V
	Standby	2.4		5.5	
Supply voltage, V_{SS}			0		V
High-level input voltage, V_{IH}		2		5.5	V
Low-level input voltage, V_{IL} (see Note 2)		–1		0.8	V
Operating free-air temperature, T_A		0		70	°C

NOTE 2: The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	High level voltage	I_{OH} = –1.0 mA	V_{CC} = 4.5 V		2.4			V
V_{OL}	Low level voltage	I_{OL} = 3.2 mA	V_{CC} = 4.5 V				0.4	V
I_I	Input current	V_I = 0 V to 5.5 V					10	μA
I_{OZ}	Off-state output current	S at 2 V or W at 0.8 V	V_O = 0 V to 5.5 V				±10	μA
I_{CC}	Supply current from V_{CC}	I_O = 0 mA, T_A = 0°C (worst case)	TMS 4044	V_{CC} = MAX		65	80	mA
				V_{CC} = 2.4 V		45	65	
			TMS 40L44	V_{CC} = MAX		40	50	
				V_{CC} = 2.4 V		30	40	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz					8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz					8	pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended supply voltage range, T_A = 0°C to 70°C 1 Series 74 TTL load, C_L = 100 pF

PARAMETER		TMS 4044-15 TMS 40L44-15		TMS 4044-20 TMS 40L44-20		TMS 4044-25 TMS 40L44-25		TMS 4044-45 TMS 40L44-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		250		450		ns
$t_{c(wr)}$	Write cycle time	150		200		250		450		ns
$t_{c(RW)}$	Read-modify-write cycle time	250		320		370		650		ns
$t_{w(W)}$	Write pulse width	80		100		100		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	80		100		100		200		ns
$t_{su(D)}$	Data set up time	80		100		100		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{h(A)}$	Address hold time	0		0		0		0		ns

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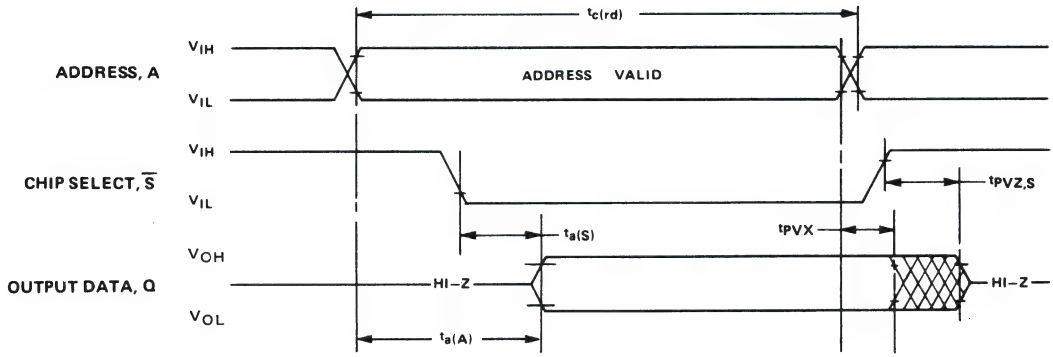
switching characteristics over recommended voltage range, T_A = 0°C to 70°C 1 Series 74 TTL load, C_L = 100 pF

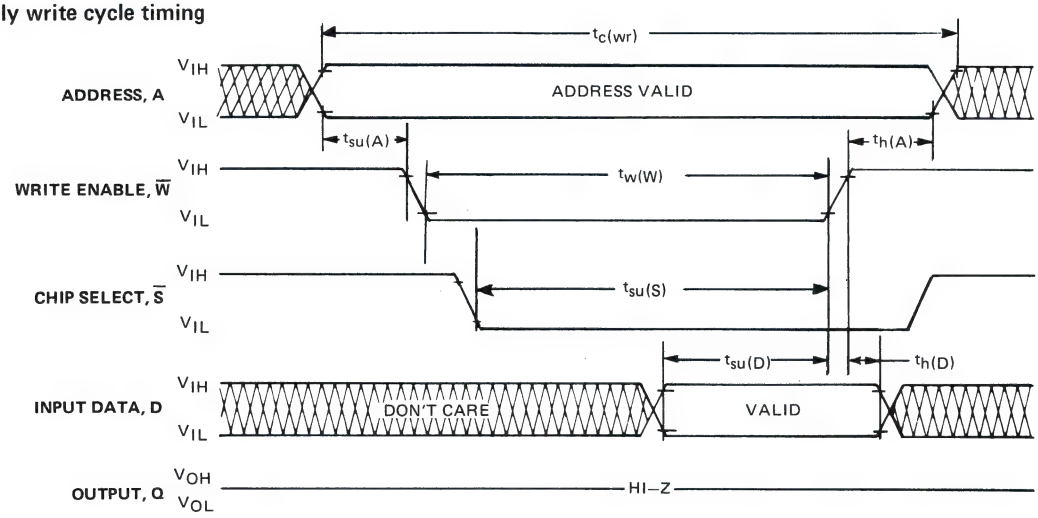
PARAMETER		TMS 4044-15 TMS 40L44-15		TMS 4044-20 TMS 40L44-20		TMS 4044-25 TMS 40L44-25		TMS 4044-45 TMS 40L44-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250		450	ns
$t_{a(S)}$	Access time from chip select low		70		70		70		100	ns
$t_{a(W)}$	Access time from write enable high		70		70		70		100	ns
t_{PVX}	Output data valid after address change	20		20		20		20		ns
$t_{PVZ,S}$	Output disable time after chip select high		50		60		60		100	ns
$t_{PVZ,W}$	Output disable time after write enable low		50		60		60		100	ns

read cycle timing**

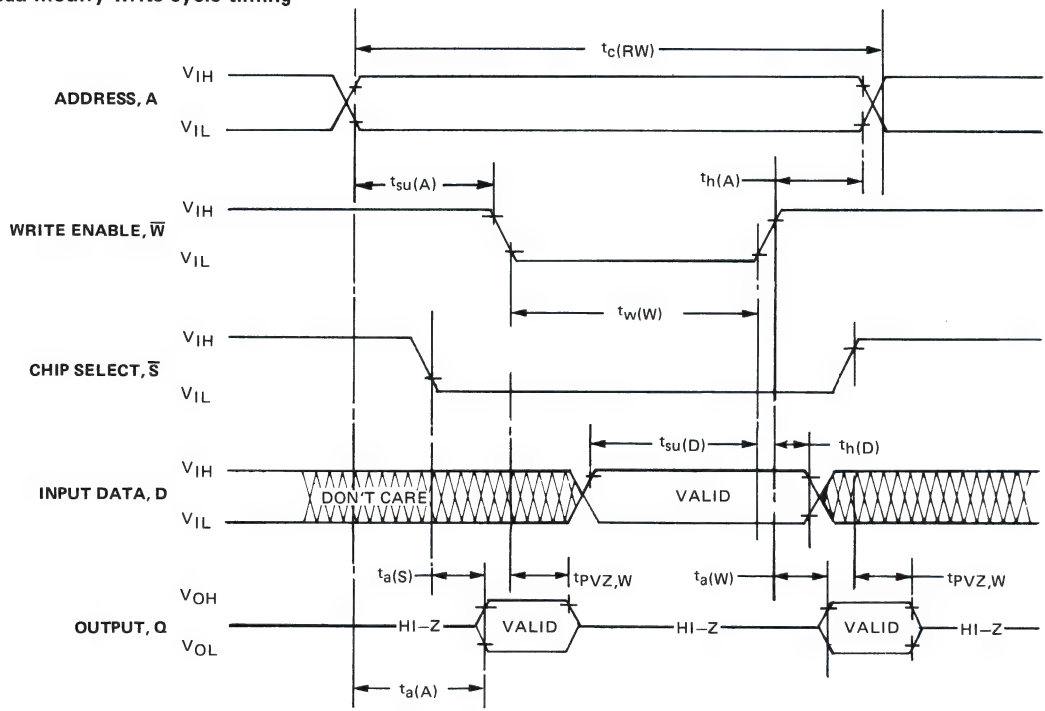


All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times = 10 ns.
**Write enable is high for a read cycle.

early write cycle timing



read-modify-write cycle timing



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TMS 2147 NL, TMS 21L47 NL
FAST 4096-WORD BY 1-BIT STATIC RAM

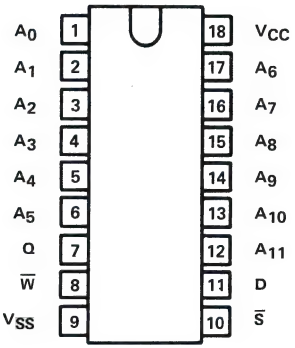
DECEMBER 1979

- 4096 X 1 Organization
- Single +5 V Supply (±10% Tolerance)
- High-Density 300-mil (7.62 mm) Packages
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- Fast . . . 3 Performance Ranges:

	ACCESS READ OR WRITE TIME (MAX)	CYCLE (MIN)
TMS 2147-5	55 ns	55 ns
TMS 2147-7/TMS 21L47-7	70 ns	70 ns

- Inputs and Outputs TTL Compatible
- Common I/O Capability
- 3-State Outputs and Chip Enable Control for OR-Tie Capability
- Automatic Chip-Select-Power-Down Operation
- Reliable SMOS (Scaled-MOS) N-Channel Technology

TMS 2147/TMS 21L47
18-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NAMES

A_0-A_{11}	Addresses
D	Data In
Q	Data Out
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

These high-speed static random-access memories are organized as 4096 words of 1 bit. Static design results in reduced overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Automatic chip select/power-down allows devices to be placed in the reduced-power mode whenever deselected.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. These 4K static RAM series are manufactured using TI's reliable state-of-the-art SMOS (scaled MOS) N-channel silicon-gate technology to optimize the cost/performance relationship.

The TMS 2147 series and the TMS 21L47 series are offered in 18-pin dual-in-line plastic (NL suffix) packages designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

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operation

addresses (A0-A11)

The twelve address inputs select one of the 4096 storage locations in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip-select/standby ($\overline{S}$)

The chip-select terminal, which can be driven directly by standard TTL circuits, affects the data-in and data-out terminals and the internal functioning of the chip itself. Whenever the chip-select terminal is low (enabled), the device is operational, input and output terminals are enabled, and data can be read or written. When the chip-select terminal is high (disabled), the device is deselected and put into a reduced-power standby mode. Data is retained during standby.

write-enable ($\overline{W}$)

The read or write mode is selected through the write-enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in (D)

Data can be written into a selected device when the write-enable input is low. The data-in terminal can be driven directly from standard TTL circuits.

data-out (Q)

The three-state output buffer provides direct TTL compatibility. The output is in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed, facilitating device operation in common I/O systems. Data-out is the same polarity as data-in.

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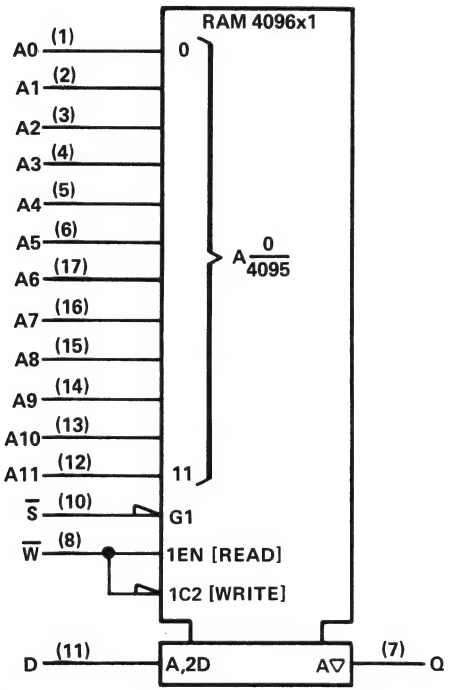
absolute maximum ratings over operating ambient temperature† range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−1.5 V to 7 V
Input voltage (any input) (see Note 1)	−1.5 V to 7 V
Continuous power dissipation	1.2 W
Operating ambient temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

logic symbol§



§ This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

FUNCTION TABLE

S	$\overline{W}$	Q	MODE
H	X	HI-Z	NOT SELECTED
L	L	HI-Z	WRITE
L	H	DATA OUT	READ

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		6	V
Low-level input voltage, V_{IL}	−1‡		0.8	V
Operating ambient temperature†, T_A	0		70	°C

† The ambient temperature conditions assume air moving perpendicular to the longitudinal axis and parallel to the seating plane of the device at a velocity of 400 feet per minute with the device under test soldered to a 4 X 6 X 0.062-inch double-sided 2-ounce copper-clad circuit board.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ The algebraic convention where the more negative limit is designated as minimum is used in this data sheet for logic voltage levels only.

NOTE 1: Voltage values are with respect to the ground terminal.

electrical characteristics over recommended operating ambient temperature† range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA, V_{CC} = 4.5 V			2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA, V_{CC} = 4.5 V					0.4	V
I_I	Input current	V_I = 0 V to 5.5 V					10	μA
I_{OZ}	Off-state output current	$\overline{S}$ at 2 V, V_O = 0 V to 4.5 V, V_{CC} = 5.5 V					±50	μA
I_{CC1}	Standby supply current from V_{CC}	$\overline{S} = V_{IH}$		TMS 2147-5		18	30	mA
				TMS 2147-7		12	20	
				TMS 21L47-7		7	10	
I_{CC2}	Operating supply current from V_{CC}	$\overline{S} = V_{IL}$, I_O = 0 mA, T_A = 0°C (worst case)	TMS 2147-5			120	180	mA
			TMS 2147-7			100	160	
			TMS 21L47-7			100	140	
I_{PO}	Peak power-on current (see Note 2)	V_{CC} = GND to V_{CC} min, $\overline{S}$ = lower of V_{CC} or V_{IH} min		TMS 2147-5			70	mA
				TMS 2147-7			50	
				TMS 21L47-7			30	
I_{OS}	Short-circuit output current§	V_{CC} = 5.5 V, V_O = GND to V_{CC}					±120	mA
C_i	Input capacitance	V_I = 0 V, f = 1 MHz					5	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz					6	pF

ac test conditions

Input pulse levels	GND to 3.5 volts
Input rise and fall times	10 ns
Input and output timing reference levels	1.5 volts
Output loading	See Figure 1

timing requirements over recommended supply voltage range and operating ambient temperature† range

PARAMETER		TMS 2147-5		TMS 2147-7 TMS 21L47-7		UNIT
		MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	55		70		ns
$t_{c(wr)}$	Write cycle time	55		70		ns
$t_{w(W)}$	Write pulse width	35		40		ns
$t_{su(A)}$	Address setup time	0		0		ns
$t_{su(S)}$	Chip select setup time	45		55		ns
$t_{su(D)}$	Data setup time	25		30		ns
$t_{h(D)}$	Data hold time	10		10		ns
$t_{h(A)}$	Address hold time	10		15		ns
t_{AVWH}	Address valid to write enable high	45		55		ns

† The ambient temperature conditions assume air moving at a velocity of 400 feet per minute.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Duration of the short-circuit should not exceed one minute.

NOTE 2: I_{PO} exceeds I_{CC1} maximum during power on, as shown in Figure 4. All pull-up resistor to V_{CC} on the S input is required to keep the device deselected; otherwise, power-on current approaches I_{CC2}.

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switching characteristics over recommended supply voltage range and operating ambient temperature† range

PARAMETER		TEST CONDITIONS	TMS 2147-5		TMS 2147-7 TMS 21L47-7		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address	R_L = 510 Ω, C_L = 30 pF, See Figure 1		55		70	ns
$t_{a(S)1}$	Access time from chip select (see Note 3)			55		70	ns
$t_{a(S)2}$	Access time from chip select (see Note 4)			65		80	ns
t_{PVX}	Output data valid after address change		5		5		ns
$t_{PVZ(w)}$	Output disable time from write enable			30		35	ns
$t_{PZV(W)}$	Output enable time from write enable		0		0		ns
$t_{PVZ(S)}$	Output disable time from chip select			40		40	ns
$t_{PZV(S)}$	Output enable time from chip select		10		10		ns
t_{pwrdn}	Power down time from chip select			30		30	ns

† The ambient temperature conditions assume air moving at a velocity of 400 feet per minute.

NOTES: 3. Chip deselected for more than 55 ns prior to selection.
4. Chip deselected for less than 55 ns prior to selection. (If the deselect time is 0 ns, the chip is by definition selected and access time occurs according to read cycle).

PARAMETER MEASUREMENT INFORMATION

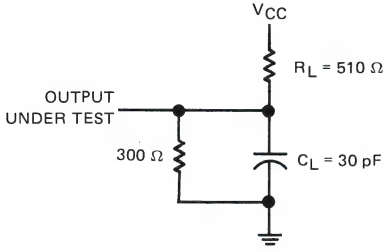
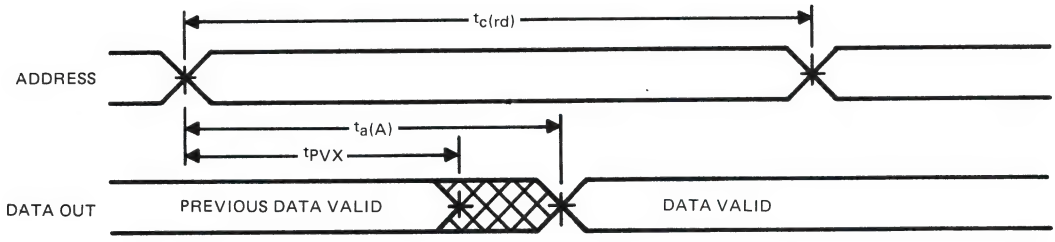


FIGURE 1 – LOAD CIRCUIT

TYPICAL DC AND AC CHARACTERISTICS

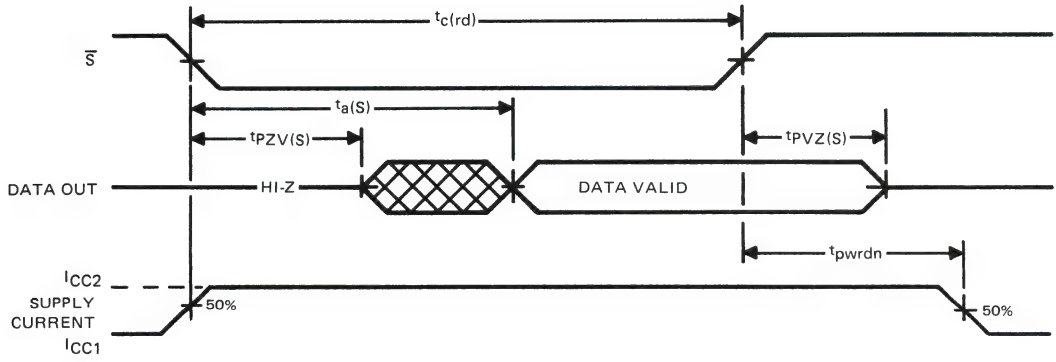
read cycle timing

from address



$\overline{W}$ is high, $\overline{S}$ is low.

from chip select



$\overline{W}$ is high, address is valid prior to or simultaneously with the high-to-low transition of $\overline{S}$.

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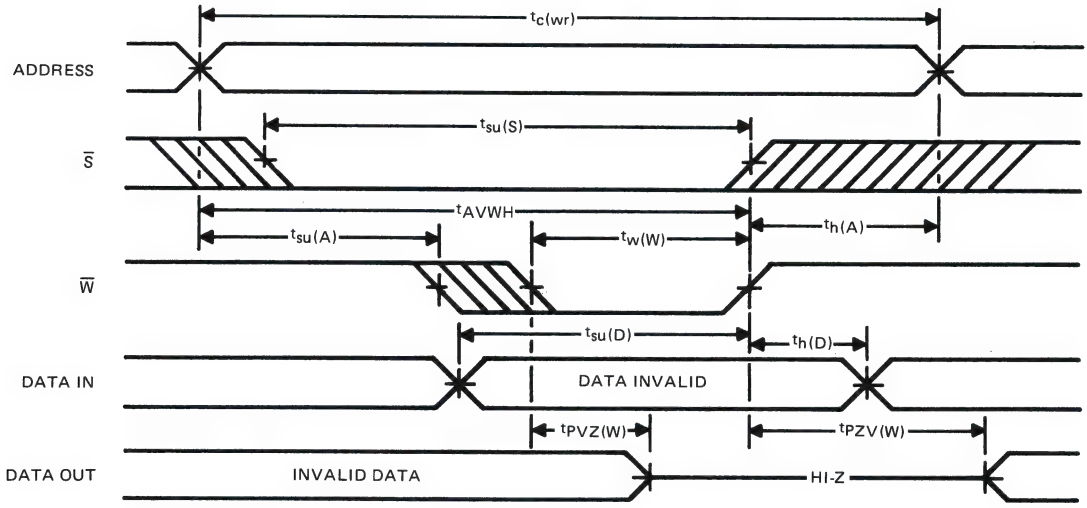
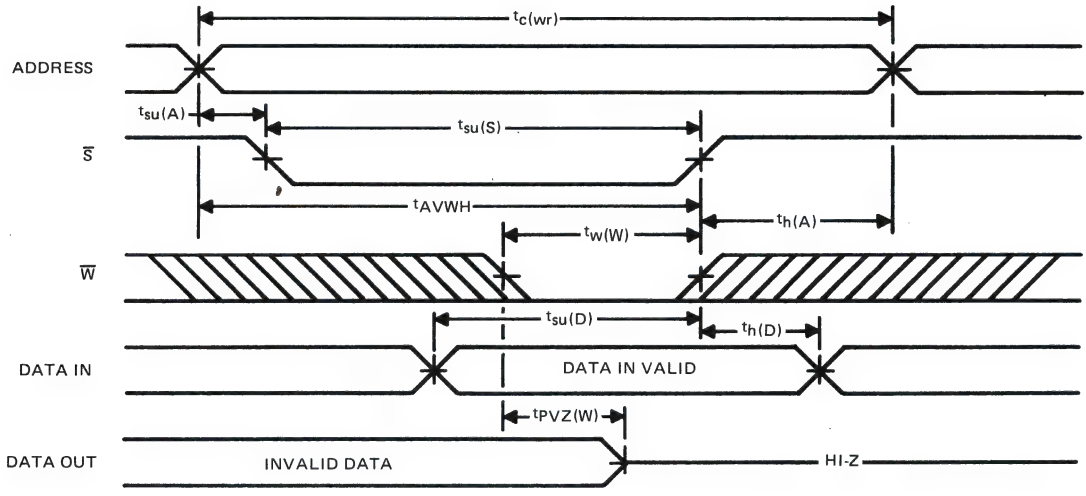
TYPICAL DC AND AC CHARACTERISTICS

write cycle timng

controlled by write enable



controlled by chip select



NOTE: If $\overline{S}$ goes high simultaneously with $\overline{W}$ high, the output remains in the high-impedance state.

TYPICAL CHARACTERISTICS

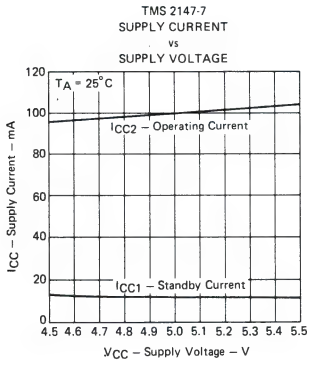


FIGURE 2

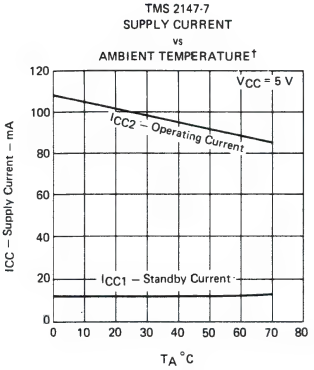


FIGURE 3

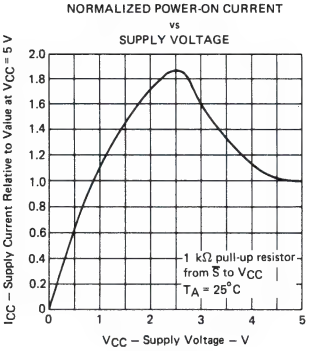

NORMALIZED POWER-ON CURRENT
vs
SUPPLY VOLTAGE
1 kΩ pull-up resistor from S̄ to V_{CC}
T_A = 25°C
I_{CC} – Supply Current Relative to Value at V_{CC} = 5 V
V_{CC} – Supply Voltage – V

FIGURE 4

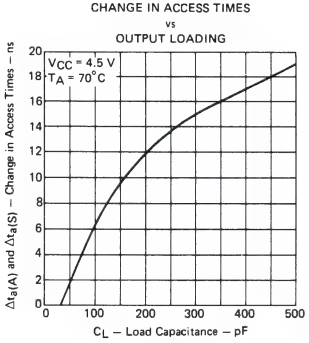

CHANGE IN ACCESS TIMES
vs
OUTPUT LOADING
V_{CC} = 4.5 V
T_A = 70°C
$\Delta t_{a(A)}$ and $\Delta t_{a(S)}$ – Change in Access Times – ns
C_L – Load Capacitance – pF

FIGURE 5

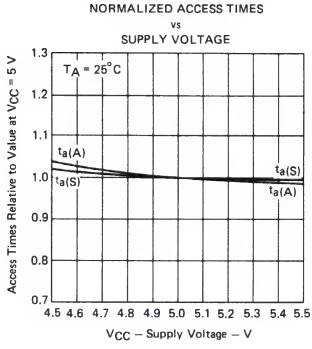


FIGURE 6

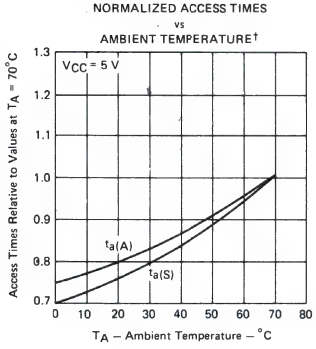


FIGURE 7

† The ambient temperature conditions assume air moving at a velocity of 400 feet per minute.

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TMS 2114 NL; TMS 2114L NL
1024-WORD BY 4-BIT STATIC RAMS

DECEMBER 1979

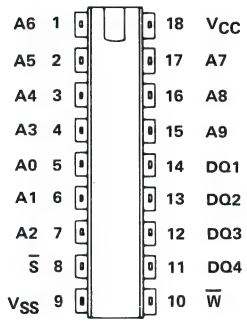
- Previously Called TMS 4045/TMS 40L45
- 1024 X 4 Organization
- Single +5 V Supply
- High Density 300-mil (7.62 mm) 18-Pin Package
- Fully Static Operation (No Clocks, No Refresh, No Timing Strobe)
- 4 Performance Ranges:

	ACCESS READ OR WRITE TIME (MAX)	CYCLE (MIN)
TMS 2114-15, TMS 2114L-15	150 ns	150 ns
TMS 2114-20, TMS 2114L-20	200 ns	200 ns
TMS 2114-25, TMS 2114L-25	250 ns	250 ns
TMS 2114-45, TMS 2114L-45	450 ns	450 ns

- 400-mV Guaranteed DC Noise Immunity with Standard TTL Loads — No Pull-Up Resistors Required
- Common I/O Capability
- 3-State Outputs and Chip Select Control for OR-Tie Capability
- Fan-Out to 2 Series 74, 1 Series 74S, or 8 Series 74LS TTL Loads
- Low Power Dissipation

	MAX (OPERATING)	MAX (STANDBY)
TMS 2114	550 mW	170 mW
TMS 2114L	330 mW	110 mW

TMS 2114/TMS 2114L
18-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NAMES

A0-A9	Addresses
DQ	Data In/Data Out
$\overline{S}$	Chip Select
V_{CC}	+5 V Supply
V_{SS}	Ground
$\overline{W}$	Write Enable

description

This series of static random-access memories is organized as 1024 words of 4 bits each. Static design results in reducing overhead costs by elimination of refresh-clocking circuitry and by simplification of timing requirements. Because this series is fully static, chip select may be tied low to further simplify system timing. Output data is always available during a read cycle.

All inputs and outputs are fully compatible with Series 74, 74S or 74LS TTL. No pull-up resistors are required. This 4K Static RAM series is manufactured using TI's reliable N-channel silicon-gate technology to optimize the cost/performance relationship. Sub 450 ns max access versions are characterized to retain data at V_{CC} = 2.4 V to reduce power dissipation.

The TMS 2114/2114L series is offered in the 18-pin dual-in-line plastic (NL suffix) package designed for insertion in mounting-hole rows on 300-mil (7.62 mm) centers. The series is guaranteed for operation from 0°C to 70°C.

operation

addresses (A0-A11)

The ten address inputs select one of the 1024 4-bit words in the RAM. The address inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in and data-out terminals. When chip select is at a logic low level, both terminals are enabled. When chip select is high, data-in is inhibited and data-out is in the floating or high-impedance state.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ or $\overline{S}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1-DQ4)

Data can be written into a selected device when the write enable input is low. The DQ terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of two Series 74 TTL gates, one Series 74S TTL gate, or eight Series 74LS TTL gates. The DQ terminals are in the high-impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

standby operation (TMS 2114/TMS 2114L-15, -20, -25)

The standby mode, which will retain data while reducing power consumption, is attained by reducing the V_{CC} supply from 5 volts to 2.4 volts. When reducing supply voltage during the standby mode, $\overline{S}$ and $\overline{W}$ must be held high to retain data. The V_{CC} transition rate must not exceed 26 mV/ms. During standby operation, data can not be read or written into the memory. When resuming normal operation, five cycle times must be allowed after normal supplies are returned for the memory to resume steady state operating conditions.

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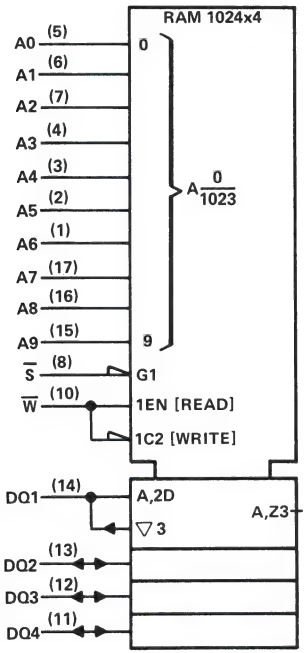
absolute maximum ratings over operating free-air temperature (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) . . . . . –0.5 to 7 V
Input voltage (any input) (see Note 1) . . . . . –1 to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –55°C to 150°C

NOTE 1: Voltage values are with respect to the ground material.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



FUNCTION TABLE

$\overline{W}$	$\overline{S}$	$\overline{OE}$	DQ1-DQ4	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER		TMS 2114-15, TMS 2114L-15 TMS 2114-20, TMS 2114L-20 TMS 2114-25, TMS 2114L-25			TMS 2114-45, TMS 2114L-45			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Operating	4.5	5	5.5	4.75	5	5.25	V
	Standby	2.4		5.5	Not applicable			
Supply voltage, V_{SS}			0			0		V
High-level input voltage, V_{IH}		2		5.5	2		5.25	V
Low-level input voltage, V_{IL} (see Note 2)		–1		0.8	–0.3		0.8	V
Operating free-air temperature, T_A		0		70	0		70	°C

NOTE 2: The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{OH}	High level voltage	I_{OH} = −1 mA**	V_{CC} = MIN (operating)		2.4			V
V_{OL}	Low level voltage	I_{OL} = 3.2 mA**	V_{CC} = MIN (operating)				0.4	V
I_I	Input current	V_I = 0 V to MAX					10	μA
I_{OZ}	Off-state output current	$\overline{S}$ at 2 V or $\overline{W}$ at 0.8 V	V_O = 0 V to MAX				±10	μA
I_{CC}	Supply current from V_{CC}	I_O = 0 mA, T_A = 0°C (worst case)	TMS 2114	V_{CC} = MAX		90	100	mA
				V_{CC} = 2.4 V*		60	70	
			TMS 2114L	V_{CC} = MAX		50	60	
				V_{CC} = 2.4 V*		35	45	
C_i	Input capacitance	V_I = 0 V, f = 1 MHz					8	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz					8	pF

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
* TMS 2114/TMS 2114L-15, -20, -25 only.
** TMS 2114/TMS 2114L-45: I_{OH} = −200 μA, I_{OL} = 2 mA.

timing requirements over recommended supply voltage range, T_A = 0°C to 70°C 1 Series 74 TTL load C_L = 100 pF

PARAMETER		TMS 2114-15 TMS 2114L-15		TMS 2114-20 TMS 2114L-20		TMS 2114-25 TMS 2114L-25		TMS 2114-45 TMS 2114L-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time	150		200		250		450		ns
$t_{c(wr)}$	Write cycle time	150		200		250		450		ns
$t_{w(W)}$	Write pulse width	80		100		100		200		ns
$t_{su(A)}$	Address set up time	0		0		0		0		ns
$t_{su(S)}$	Chip select set up time	80		100		100		200		ns
$t_{su(D)}$	Data set up time	80		100		100		200		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{h(A)}$	Address hold time	0		0		0		20		ns

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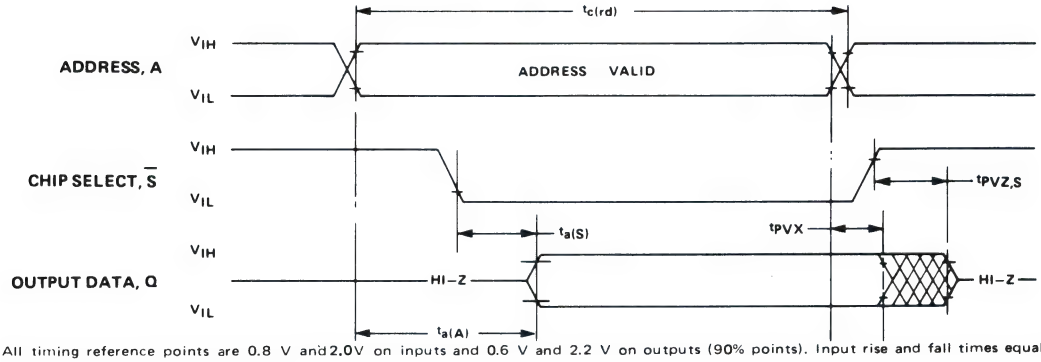
switching characteristics over recommended voltage range, T_A = 0°C to 70°C, 1 Series 74 TTL load, C_L = 100 pF

PARAMETER		TMS 2114-15 TMS 2114L-15		TMS 2114-20 TMS 2114L-20		TMS 2114-25 TMS 2114L-25		TMS 2114-45 TMS 2114L-45		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(A)}$	Access time from address		150		200		250		450	ns
$t_{a(S)}$	Access time from chip select (or output enable) low		70		85		100		120	ns
$t_{a(W)}$	Access time from write enable high		70		85		100		120	ns
t_{PVX}	Output data valid after address change	20		20		20		20		ns
$t_{PVZ,S}$	Output disable time after chip select (or output enable) high		50		60		60		100	ns
$t_{PVZ,W}$	Output disable time after write enable low		50		60		60		100	ns

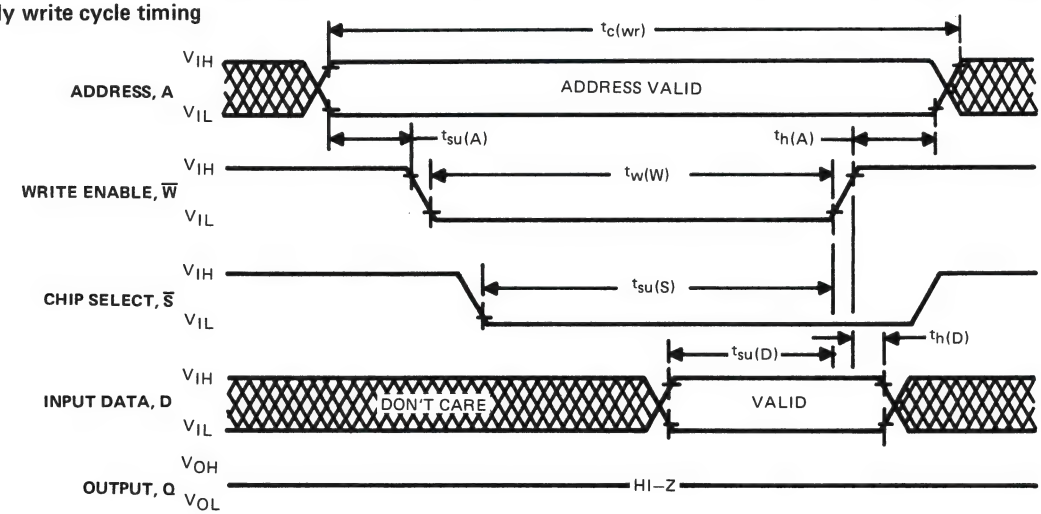
read cycle timing**



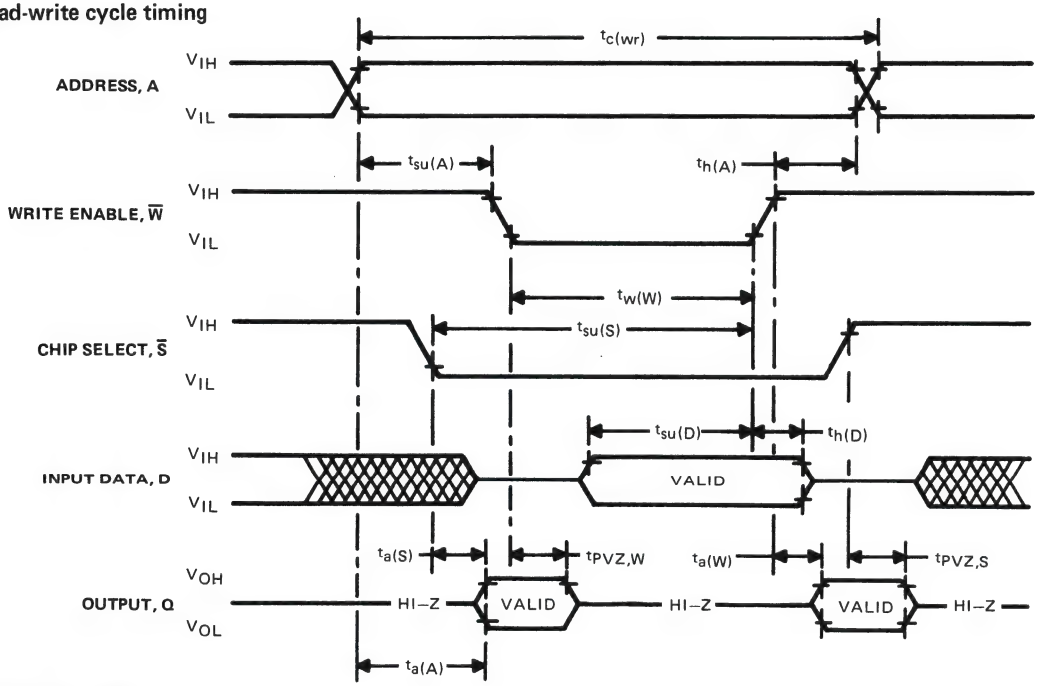
All timing reference points are 0.8 V and 2.0V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

**Write enable is high for a read cycle.

early write cycle timing



read-write cycle timing



applications data

Early write cycle avoids DQ conflicts by controlling the write time with $\overline{S}$. On the diagram above, the write operation will be controlled by the leading edge of $\overline{S}$, not $\overline{W}$. Data can only be written when both $\overline{S}$ and $\overline{W}$ are low. Either $\overline{S}$ or $\overline{W}$ being high inhibits the write operation. To prevent erroneous data being written into the array, the addresses must be stable during the write cycle as defined by $t_{su(A)}$, $t_{w(W)}$, and $t_{h(A)}$.

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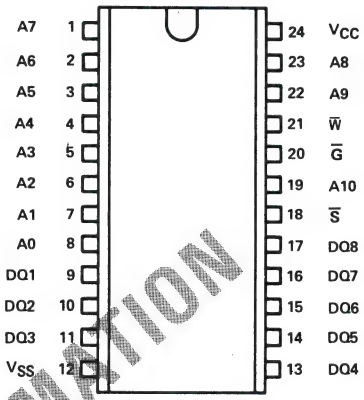
TMS 4016 NL
2048-WORD BY 8-BIT STATIC RAM

DECEMBER 1979

- 2K X 8 Organization
- Single +5 V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600 (15.2 mm) Mil Package Configuration
- Plug-in Compatible with 16K 5 V EPROMs
- 8-Bit Output for Use in Microprocessor-Based Systems
- Max Access/Min Cycle . . . 450 ns
- Tri-State Outputs with $\overline{S}$ for Or-ties
- $\overline{G}$ Eliminates Need for External Bus Buffers
- Common I/O Capability
- All Inputs and Outputs Fully TTL Compatible
- Fanout to Series 74, Series 74S, or Series 74LS TTL Loads
- N-Channel Silicon-Gate Technology
- Power Dissipation Under 475 mW Max
- Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads

TMS 4016
24-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0-A10	Addresses
DQ1-DQ8	Data In/Data Out
$\overline{S}$	Chip Select
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{SS}	Ground
V_{CC}	+5 V Supply

ADVANCE INFORMATION

description

The TMS 4016 static random-access memory is organized as 2048 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS 4016 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS 4016 static RAM has the same standardized pinout as TI's compatible EPROM family. This, along with other compatible features, makes the TMS 4016 plug-in compatible with the TMS 2516 (or other 16K 5 V EPROMs). Minimal, if any modifications are needed. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

The TMS 4016 is offered in the plastic (NL suffix) 24-pin dual-in-line package designed for insertion in mounting hole rows on 600-mil (15.2 mm) centers. It is guaranteed for operation from 0°C to 70°C.

TURN TO PAGE 93 FOR EXPLANATION OF TMS 4016–16K 5V EPROM COMPATIBILITY.

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operation

addresses (A0-A10)

The eleven address inputs select one of the 2048 8-bit words in the RAM. The address-inputs must be stable for the duration of a write cycle. The address inputs can be driven directly from standard Series 54/74 TTL with no external pull-up resistors.

output enable ($\overline{G}$)

The output enable terminal, which can be driven directly from standard TTL circuits, affects only the data-out terminals. When output enable is at a logic high level, the output terminals are disabled to the high-impedance state. Output enable provides greater output control flexibility, simplifying data bus design.

chip select ($\overline{S}$)

The chip-select terminal, which can be driven directly from standard TTL circuits, affects the data-in/data-out terminals. When chip select and output enable are at a logic low level, the D/Q terminals are enabled. When chip select is high, the D/Q terminals are in the floating or high-impedance state and the input is inhibited.

write enable ($\overline{W}$)

The read or write mode is selected through the write enable terminal. A logic high selects the read mode; a logic low selects the write mode. $\overline{W}$ must be high when changing addresses to prevent erroneously writing data into a memory location. The $\overline{W}$ input can be driven directly from standard TTL circuits.

data-in/data-out (DQ1-DQ8)

Data can be written into a selected device when the write enable input is low. The D/Q terminal can be driven directly from standard TTL circuits. The three-state output buffer provides direct TTL compatibility with a fan-out of one Series 74 TTL gate, one Series 74S TTL gate, or five Series 74LS TTL gates. The D/Q terminals are in the high impedance state when chip select ($\overline{S}$) is high or whenever a write operation is being performed. Data-out is the same polarity as data-in.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.5 to 7 V
Input voltage (any input) (see Note 1)	−0.5 to 7 V
Continuous power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

NOTE 1: Voltage values are with respect to the ground terminal.

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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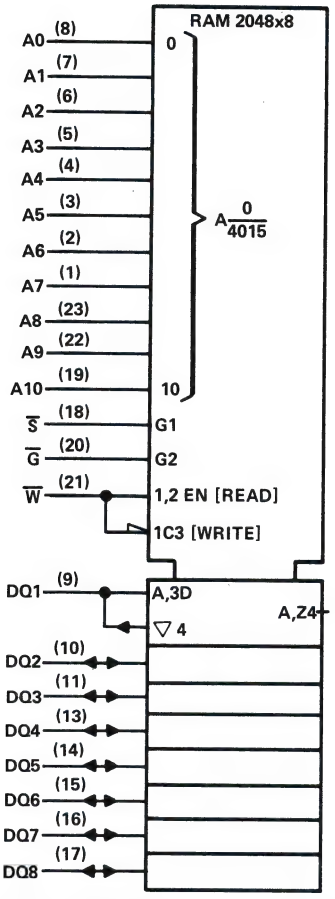
logic symbol†



W	S	G	DQ1-DQ8	MODE
L	L	X	VALID DATA	WRITE
H	L	L	DATA OUTPUT	READ
X	H	X	HI-Z	DEVICE DISABLED
H	L	H	HI-Z	OUTPUT DISABLED

†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		5.25	V
Low-level input voltage, V_{IL}	−1		0.8	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High level voltage	I_{OH} = –200 μA	V_{CC} = 4.75 V	2.4			V
V_{OL}	Low level voltage	I_{OL} = 2 mA	V_{CC} = 4.75 V			0.4	V
I_I	Input current	V_I = 0 V to 5.25 V				10	μA
I_{OZ}	Off-state output current	$\overline{CS}$ or $\overline{OE}$ at 2 V or $\overline{W}$ at 0.8 V	V_O = 0 to 5.25 V			10	μA
I_{CC}	Supply current from V_{CC}	I_O = 0 mA, T_A = 0°C (worst case)	V_{CC} = 5.25 V		65	90	mA
C_i	Input capacitance	V_I = 0 V,	f = 1 MHz			8	pF
C_o	Output capacitance	V_O = 0 V,	f = 1 MHz			12	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

timing requirements over recommended supply voltage range and operating free-air temperature range

PARAMETER		MIN	MAX	UNIT
$t_{c(rd)}$	Read cycle time	450		ns
$t_{c(wr)}$	Write cycle time	450		ns
$t_{w(W)}$	Write pulse width	400		ns
$t_{su(A)}$	Address set-up time	0		ns
$t_{su(S)}$	Chip select set up time	400		ns
$t_{su(D)}$	Data setup time	400		ns
$t_{h(A)}$	Address hold time	0		ns
$t_{h(D)}$	Data hold time	0		ns
$t_{T(A)}$	Address transition time	5	100	ns
t_{GHWL}	Time interval, output enable high before write low	0		ns
t_{WLSL}	Time interval, write low before chip select low	0		ns
t_{WHGL}	Time interval, write high before output enable low	0		ns
t_{GLSH}	Time interval, output enable low before chip select high	0		ns

switching characteristics over recommended voltage range, T_A = 0°C to 70°C, 1 series 74 TTL load, C_L = 100 pF

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address			450	ns
$t_{a(S)}$	Access time from chip select low			150	ns
$t_{a(G)}$	Access time from output enable low			150	ns
t_{PVX}	Output data valid after address change	10	80		ns
$t_{PVZ,S}$	Output disable time after chip select high			120	ns
$t_{PVZ,G}$	Output disable time after output enable high			120	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

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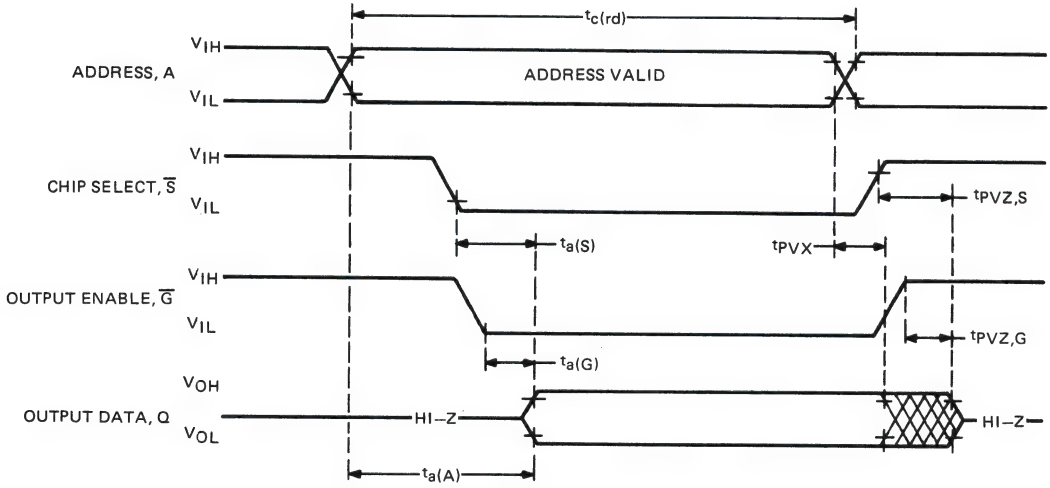
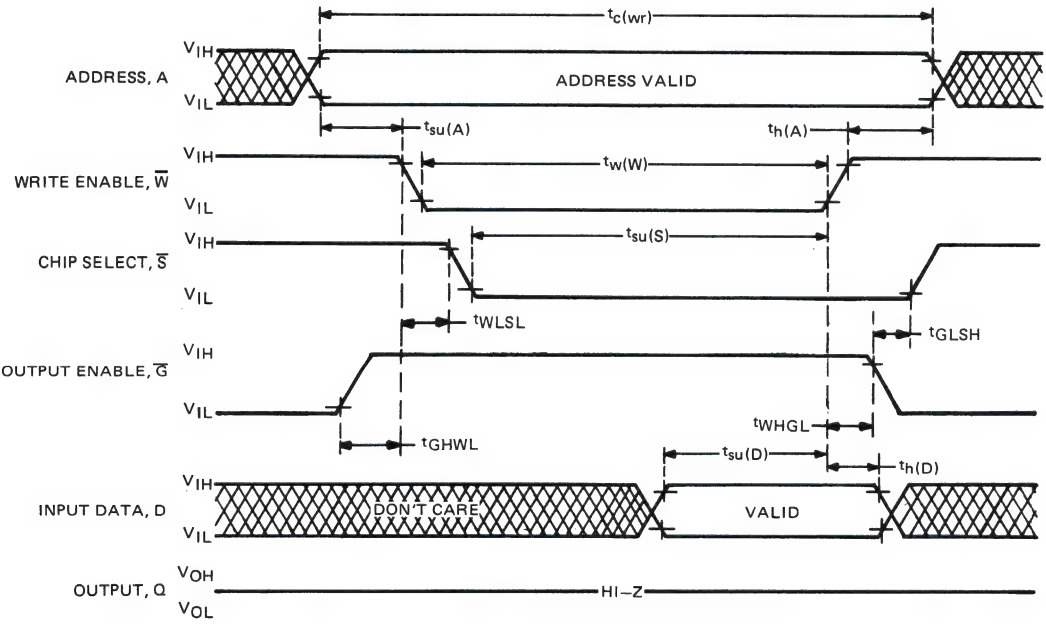
read cycle timing**



All timing reference points are 0.8 V and 2.0 V on inputs and 0.6 V and 2.2 V on outputs (90% points). Input rise and fall times equal 10 nanoseconds.

** Write enable is high for a read cycle.

early write cycle timing



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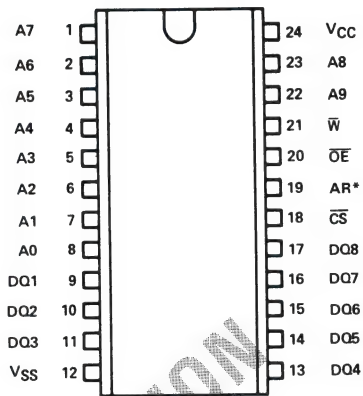
TMS 4008 NL
1024-WORD BY 8-BIT STATIC RAM

DECEMBER 1979

- 1K X 8 Organization
- Single +5 V Supply
- Fully Static Operation (No Clocks, No Refresh)
- JEDEC Standard Pinout
- 24-Pin 600 (15.2 mm) Mil Package Configuration
- Plug-in Compatible with 8K 5 V EPROMs
- 8-Bit Output for Use in Microprocessor-Based Systems
- Max Access . . . 450 ns
- Tri-State Outputs with $\overline{CS}$ for OR-Ties
- $\overline{OE}$ Eliminates Need for External Bus Buffers
- Common I/O Capability
- All Inputs and Outputs Fully TTL Compatible
- Fanout to Series 74, Series 74S, or Series 74LS TTL Loads
- N-Channel Silicon-Gate Technology
- Power Dissipation Under 475 mW Max
- Guaranteed dc Noise Immunity of 400 mV with Standard TTL Loads

TMS 4008
24-PIN PLASTIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



* AR tied to V_{IL} if TMS 4008-NL0
V_{IH} if TMS 4008-NL1

PIN NOMENCLATURE	
A0-A9	Addresses
AR	Array Select
DQ1-DQ8	Data In/Data Out
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{W}$	Write Enable
V_{SS}	Ground
V_{CC}	+5 V Supply

ADVANCE INFORMATION

description

The TMS 4008 static random-access memory is organized as 1024 words of 8 bits each. Fabricated using proven N-channel, silicon-gate MOS technology, the TMS 4008 operates at high speeds and draws less power per bit than 4K static RAMs. It is fully compatible with Series 74, 74S, or 74LS TTL. Its static design means that no refresh clocking circuitry is needed and timing requirements are simplified. Access time is equal to cycle time. A chip select control is provided for controlling the flow of data-in and data-out and an output enable function is included in order to eliminate the need for external bus buffers.

Of special importance is that the TMS 4008 static RAM has the same standardized pinout as TI's compatible EPROM family. Minimal, if any modifications are needed. This allows the microprocessor system designer complete flexibility in partitioning his memory board between read/write and non-volatile storage.

The TMS 4008 is offered in the plastic (NL suffix) 24-pin dual-in-line package designed for insertion in mounting hole rows on 600-mil (15.2 mm) centers. It is guaranteed for operation from 0°C to 70°C.

COMPLETE INFORMATION MAY BE OBTAINED FROM YOUR LOCAL TI SALES OFFICE OR AUTHORIZED DISTRIBUTOR LISTED NEAR THE FRONT OF THIS DATA BOOK.

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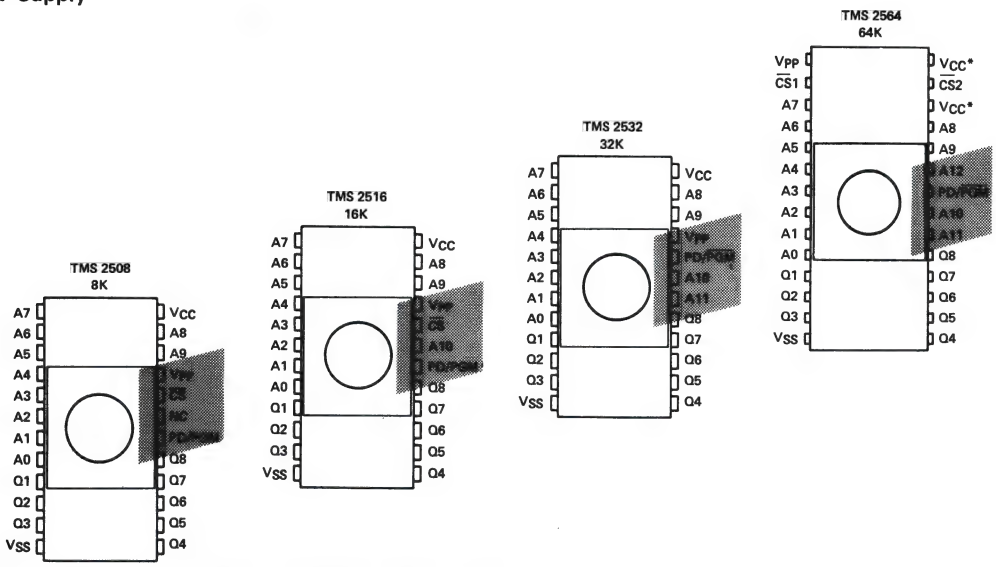
EPROM DATA SHEETS

EPROM COMPATIBILITY

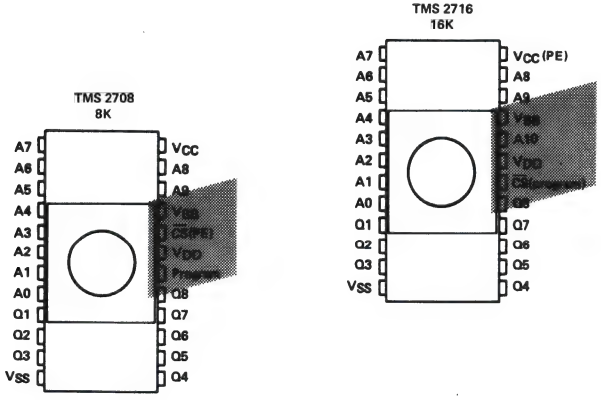
All TI EPROMs are pin compatible with each other and with industry standard ROMs. TI EPROMs fall into two general categories: single +5 V power supply and triple supply (+12, +5, –5 V). +5 V EPROMs range in density from 8K to 64K; triple supply devices from 8K to 16K. Pinouts for these devices are shown below.

+5 V Supply


TMS 2508
8K
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC A8 A9 VPP CS RC PD/PGM Q8 Q7 Q6 Q5 Q4
TMS 2516
16K
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC A8 A9 VPP CS A10 PD/PGM Q8 Q7 Q6 Q5 Q4
TMS 2532
32K
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC A8 A9 VPP PD/PGM A10 A11 Q8 Q7 Q6 Q5 Q4
TMS 2564
64K
VPP CS1 A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC* CS2 VCC* A8 A9 A12 PD/PGM A10 A11 Q8 Q7 Q6 Q5 Q4

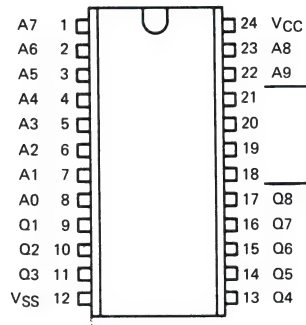
* Connected internally, V_{CC} need be supplied to only one of these two pins.

Triple Supply


TMS 2708
8K
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC A8 A9 VBB CS(PE) VDD Program Q8 Q7 Q6 Q5 Q4
TMS 2716
16K
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 VSS
VCC(PE) A8 A9 VBB A10 VDD CS(Program) Q8 Q7 Q6 Q5 Q4

Industry standard 5 V ROM pinouts are listed in the table below.

24 PIN ROM



8K	16K	32K	64K
CS/$\overline{CS}$	CS/$\overline{CS}$	CS/$\overline{CS}$	A12
CS/$\overline{CS}$	CS/$\overline{CS}$	CS/$\overline{CS}$	CS/$\overline{CS}$
CS/$\overline{CS}$	A10	A10	A10
CS/$\overline{CS}$	CS/$\overline{CS}$	A11	A11

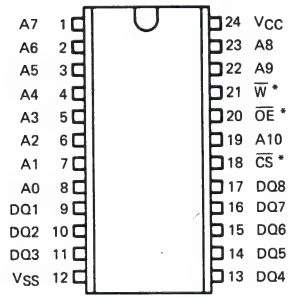
Upgrading between any two consecutive EPROM densities requires at most one jumper (if programming is done outside the system). Switching from 5 V EPROM to 5 V ROM also requires at most one jumper.

64K EPROM – 64K ROM

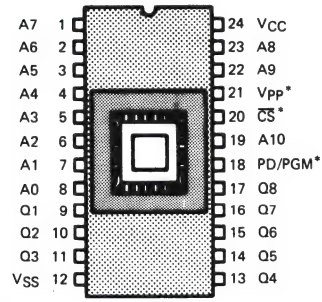
TI's 64K EPROM, the TMS 2564, bridges the gap between 24-pin and 28-pin devices. This is because the lower 24 pins of TI's 64K EPROM are identical to the industry standard 64K ROM. Once the 28-pin socket is designed in, switching from EPROM to ROM is straight forward. Upgrading from 32K EPROM to the TMS 2564 is just as simple once the 28-pin socket is reserved.

RAM - EPROM COMPATIBILITY
TMS 4016 - TMS 2516

TMS 4016
2K X 8 STATIC RAM



TMS 2516
2K X 8 5V EPROM



*These pins though apparently different are compatible when switching to the TMS 2516.

Memory boards may now be designed with essentially one pinout type, leaving read/write versus read-only partitioning decisions until later. TI's TMS 4016 static RAM is plug-compatible with 16K 5 V EPROMs. Extensive compatibility exists between the TMS 4016 and TMS 2516. Both the TMS 4016 and TMS 2516 have a 2K X 8 organization. Both come in 600 mil, 24-pin DIP packages. As can be seen above all addresses, data-in/data-out, and V_{SS} and V_{CC} are on the same pins on both devices. And the three other pins, 18, 20, and 21 are also compatible. Compatibility also applies to input and output currents and voltages and to timing requirements. To find out more please write: Texas Instruments, P.O. Box 1443, M/S 6965, Houston, Texas 77001, for the RAM-EPROM Compatibility Application Brief. Or call or write your nearest TI sales office or authorized distributor.

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TMS 2508 JL
FAST 1024-WORD BY 8-BIT
ERASABLE PROGRAMMABLE READ-ONLY MEMORY

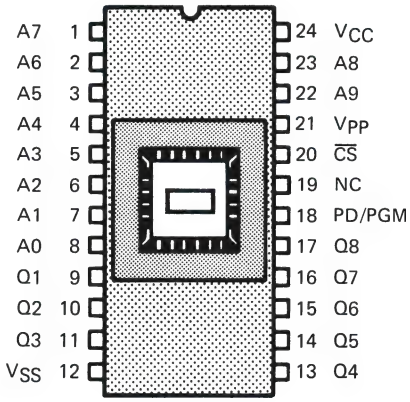
DECEMBER 1979

- **Organization . . . 1K × 8**
- **Single +5 V Power Supply**
- **Pin Compatible with Existing ROMs and EPROMs (8 K, 16 K, and 64 K)**
- **JEDEC Standard Pinouts**
- **All Inputs/Outputs Fully TTL Compatible**
- **Static Operation (No Clocks, No Refresh)**
- **Fast . . . Down to 250 ns**
- **2 Performance Ranges**

	Max Access/Min Cycle
TMS 2508-25	250 ns
TMS 2508-30	300 ns

- **8-Bit Output for Use in Microprocessor-Based Systems**
- **N-Channel Silicon-Gate Technology**
- **3-State Output Buffers**
- **Low Power**
  - **— Active . . . 250 mW Typical**
  - **— Standby . . . 50 mW Typical**
- **Guaranteed dc Noise Immunity with Standard TTL Loads**
- **No Pull-Up Resistors Required**

TMS 2508
24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address Inputs
$\overline{CS}$	Chip Select
PD/PGM	Power Down/Program
NC	No Internal Connection
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2508 is a high-speed 8192-bit, ultraviolet light erasable, electrically programmable read-only memory. It is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and Bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for OR tying multiple devices on a common bus.

Both versions operate from a single +5-V supply (in the read mode), making them ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside the system, existing 5-V EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits for the TMS 2508 is 50 seconds.

Devices are offered in a 600-mil (15.2-mm) cerpak (JL suffix) package rated for operation from 0°C to 70°C.

operation

FUNCTION	PIN	MODE					
		READ	OUTPUT DISABLE	POWER DOWN	START PROGRAMMING	INHIBIT PROGRAMMING	PROGRAM VERIFICATION
PD/PGM	18	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{CS}$	20	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP}	21	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC}	24	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q	9-11, 13-17	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more TMS 2508's are commoned on the same bus, the output of any one device in the circuit can be read with no interference from the competing outputs of the others. The TMS 2508 whose output is to be read should have a low-level TTL signal applied to the $\overline{CS}$ and PD/PGM pins. All other 2508's in the circuit should have their outputs disabled by applying a high-level signal to at least one of these same pins. (PD/PGM can be left low, but it may be advantageous to power down the device during output disable). Output data is accessed at pins Q1 to Q8. Data can be accessed in 250 or 300 ns = $t_{a(A)}$. (Access time from $\overline{CS}$ is 125 or 150 ns = $t_{a(CS)}$, once the addresses are stable).

power down

Active power dissipation can be cut by 70% by applying a high TTL signal to the PD/PGM pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2508 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12-milliwatt-per-square-centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

start programming

After erasure, logic lows are programmed into the desired locations. A low can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{CS}$ is at V_{IH}. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 50 millisecond TTL high-level Pulse should be applied to the PD/PGM pin for each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More then one TMS 2508 can be programmed when the devices are connected in parallel.

inhibit programming

When two or more TMS 2508's are connected in parallel, data can be programmed into all devices or only chosen devices. Devices not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{CS}$ pin.

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program verification

A verify is done to see if the device was programmed correctly. It can be done on each location immediately after that location is programmed and can be done at any time. To do a verify V_{PP} may be kept at +25 V.

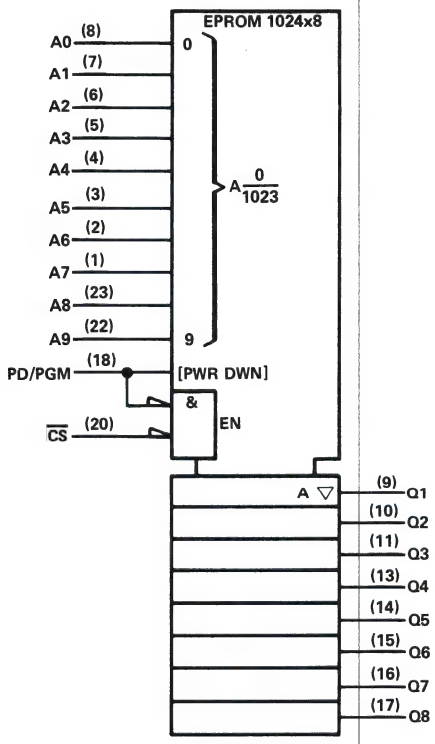
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}		V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		V_{CC}+1	V
Low-level input voltage, V_{IL}	−0.1		0.8	V
Read cycle time, $t_{c(rd)}$ For TMS 2508-25	250			ns
Read cycle time, $t_{c(rd)}$ For TMS 2508-30	300			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{CC} or V_{PP} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1V).

electrical characteristics over full range of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage*	$I_{OH} = -400\ \mu A$	2.4			V
V_{OL}	Low Level output voltage*	$I_{OL} = 2.1$ mA			0.45	V
I_I	Input current (leakage)	$V_I = 5.25$V			10	μA
I_O	Output current (leakage)	$V_O = 5.25$V			10	μA
I_{PP1}	V_{PP} supply current	$V_{PP} = 5.25$, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		10	25	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{CS}$ = PD/PGM = V_{IL}		50	85	mA

†Typical values are at $T_A = 25°C$ and nominal voltages.
*AC timing measurements made with 50% pattern and at 90% points.

capacitance over recommended supply voltage and operating free-air temperature range f = 1 MHz

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	$V_I = 0$ V, f = 1 MHz	4	6	pF
C_o	Output capacitance	$V_O = 0$ V, f = 1 MHz	8	12	pF

†All typical values are $T_A = 25°C$ and nominal voltage.

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switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTE 4)	TMS 2508-25			TMS 2508-30			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq$ 20 ns, $t_f \leq$ 20 ns		180	250		215	300	ns
$t_{a(CS)}$	Access time from chip select				125			150	ns
t_{PVX}	Output not valid from address change		0			0			ns
t_{PXZ}	Output disable time from chip deselect during read only		0		100	0		100	ns
t_{PXZ}	Output disable time from chip deselect during program and program verify				125			150	ns
t_{PXZ}	Output disable time from PD/PGM during standby		0		100	0		100	ns
$t_{a(PD)}$	Access time from power down				250			300	ns

† All typical values are at T_A = 25°C and nominal voltages.

NOTE 4. For all switching characteristics and timing measurements, input pulse levels are 0.8 V to 2.0 V and V_{PP} = 25 V ± 1 V during programming.
All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

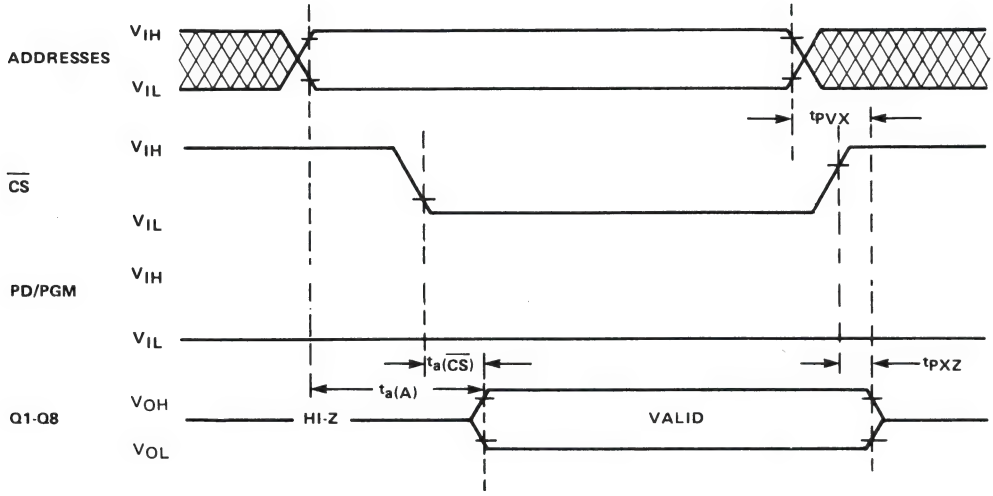
recommended timing requirements for programming T_A = 25°C (see Note 4)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(CS)}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(V_{PP})}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(CS)}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

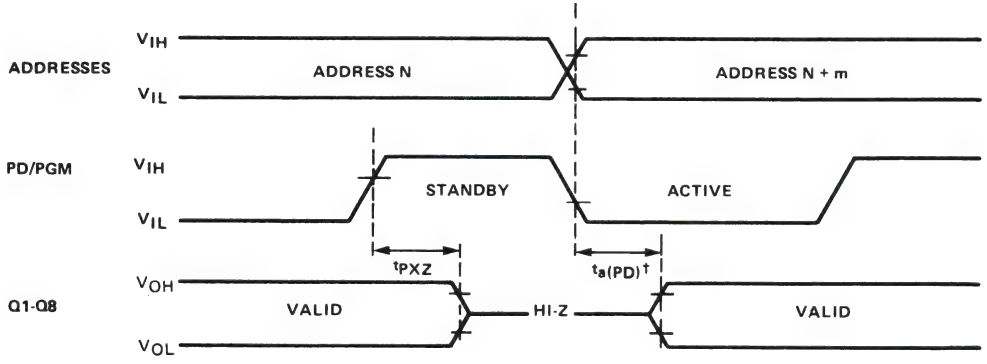
†Typical values are at nominal voltages.

NOTE 4. For all switching characteristics and timing measurements, input pulse levels are 0.8 V to 2.0 V and V_{PP} = 25 V ± 1 V during programming.
All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

read cycle timing



standby mode



NOTE: $\overline{CS}$ must be in low state during Active Mode, "Don't Care" otherwise.

†$t_{a(PD)}$ referenced to PD/PGM or the address, whichever occurs last.

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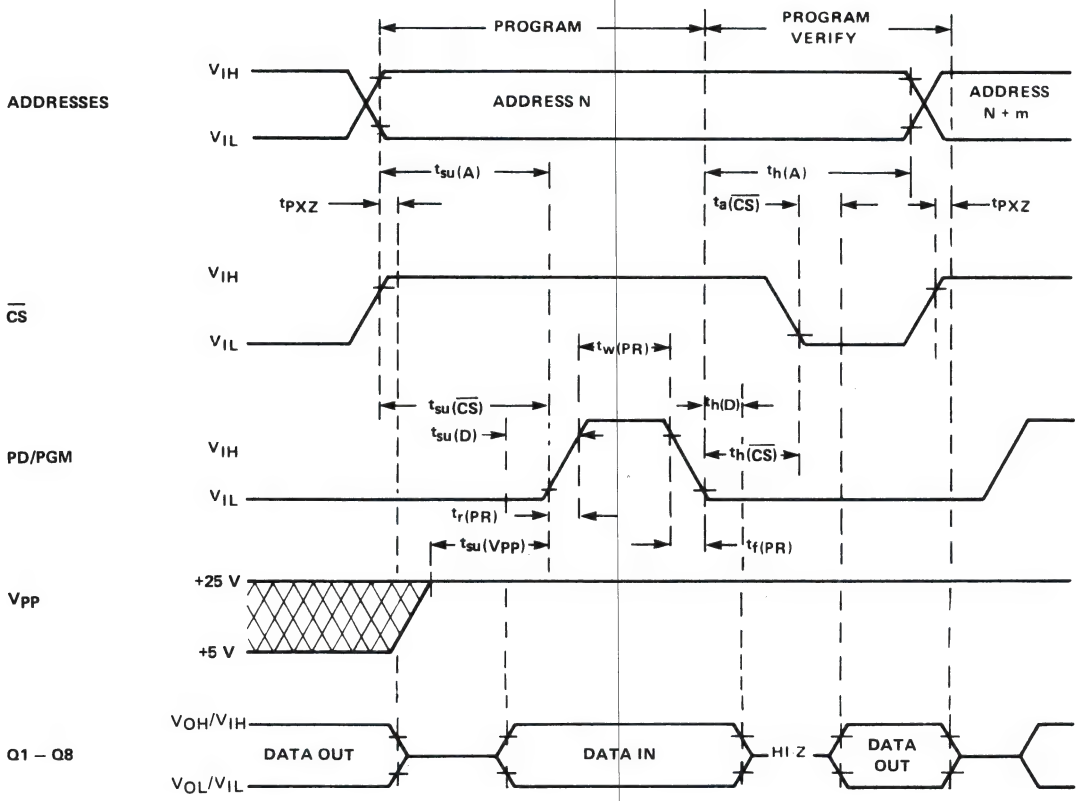
program cycle timing

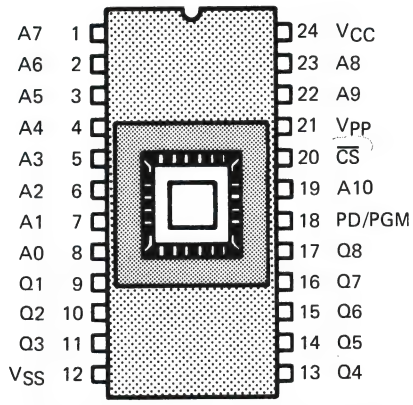


TMS 2516 JL AND TMS 2516-35 JL
16,384-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

DECEMBER 1979

- Organization . . . 2K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time
  - TMS 2516-35 . . . 350 ns
  - TMS 2516 . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power
  - Active . . . 285 mW Typical
  - Standby . . . 50 mW Typical
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$	Chip Select
PD/PGM	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2516 and TMS 2516-35 are 16,384-bit, ultraviolet-light erasable, electrically programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 2516-35 is plug-in compatible with the TMS 4016 16K static RAM. It is offered in a dual-in-line cerpak package (JL suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 100 seconds.

operation

FUNCTION (PINS)	MODE					
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming	Program Verification
PD/PGM (18)	V_{IL}	Don't Care	V_{IH}	Pulsed V_{IL} to V_{IH}	V_{IL}	V_{IL}
$\overline{CS}$ (20)	V_{IL}	V_{IH}	Don't Care	V_{IH}	V_{IH}	V_{IL}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V	+25 V (or +5 V)
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z	Q

read/output disable

When the outputs of two or more TMS 2516's and/or TMS 2516-35's are connected to the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the $\overline{CS}$ and PD/PGM pins. All other devices in the circuit should have their outputs disabled by applying high-level signal to these same pins. PD/PGM can be left low, but it may be advantageous to power down the device during output disable. Output data is accessed at pins Q1 through Q8. On the TMS 2516 data can be accessed in 450 ns and access time from $\overline{CS}$ is 150 ns. On The TMS 2516-35 data can be accessed in 350 ns and access time from $\overline{CS}$ is 120 ns. These access times assume that the addresses are stable.

power down

Active power dissipation can be cut by 80% by applying a high TTL signal to the PD/PGM pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2516 or TMS 2516-35 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12-milliwatt per-square-centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state (assuming a high-level output corresponds to logic "1").

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V and $\overline{CS}$ is at V_{IH}. Data is presented in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 50-millisecond TTL high-level pulse should be applied to the PGM pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. Several TMS 2516's and/or TMS 2516-35's can be programmed simultaneously when the devices are connected in parallel.

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inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2516's or TMS 2516-35's not intended to be programmed (i.e., inhibited) should have a low level applied to the PD/PGM pin and a high-level applied to the $\overline{CS}$ pin.

program verification

A verification is done to see if the device was programmed correctly. A verification can be done at any time. It can be done on each location immediately after that location is programmed. To do a verification, V_{PP} may be kept at +25 V.

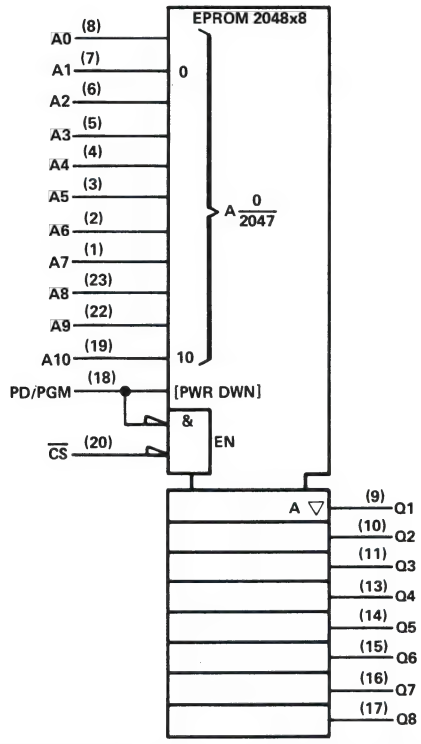
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	TMS 2516			TMS 2516-35			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2		V_{CC}+1	2		V_{CC}+1	V
Low-level input voltage, V_{IL}	–0.1		0.8	–0.1		0.8	V
Read cycle time, $t_{c(rd)}$	450			350			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage*	I_{OH} = –400 μA	2.4			V
V_{OL}	Low-level output voltage*	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 5.25 V			10	μA
I_O	Output current (leakage)	V_O = 5.25 V			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/PGM = V_{IL}			6	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/PGM = V_{IH}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/PGM = V_{IH}		10	25	mA
I_{CC2}	V_{CC} supply current (active)	$\overline{CS}$ = PD/PGM = V_{IL}		57	100	mA

†Typical values are at T_A = 25°C and nominal voltage.
*All AC and PC measurements are made at 10% and 90% points with a 50% pattern.

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz*

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

†All typical values are T_A = 25°C and nominal voltage
*Capacitive measurements are made on sample basis only

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switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS 2516			TMS 2516-35			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		280	450		250	350	ns
$t_{a(CS)}$	Access time from chip select				120			120	ns
$t_{a(PR)}$	Access time from PD/PGM			280	450		250	350	ns
t_{PVX}	Output not valid from address change,		0			0			ns
t_{PXZ}	Output disable time from chip deselect during read only		0		100	0		100	ns
t_{PXZ}	Output disable time from chip deselect during program and program verify				120			120	ns
t_{PXZ}	Output disable time from PD/PGM		0		100	0		100	ns

† All typical values are at T_A = 25°C and nominal voltages.

recommended timing requirements for programming T_A = 25°C (see Note 4)

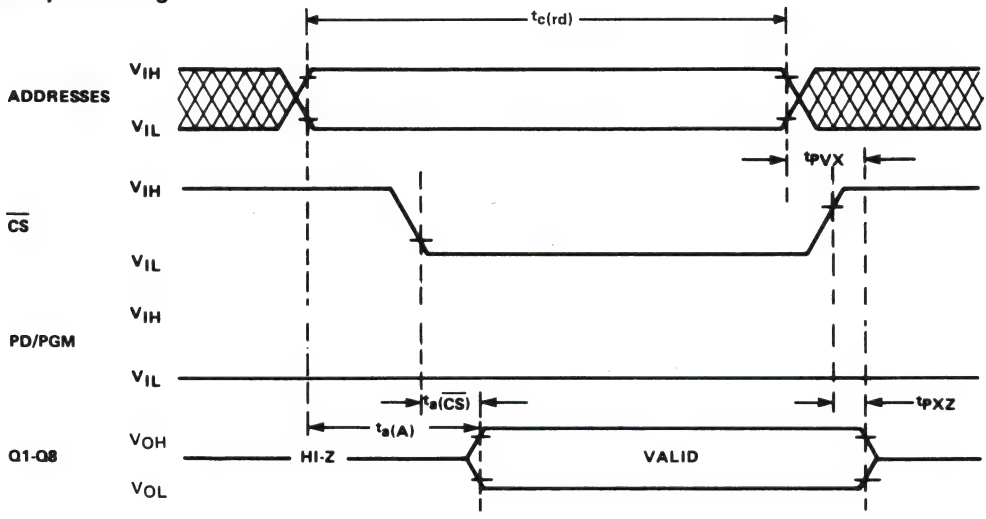
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(\overline{CS})}$	Chip-select setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(\overline{CS})}$	Chip-select hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs

†Typical values are at nominal voltages.

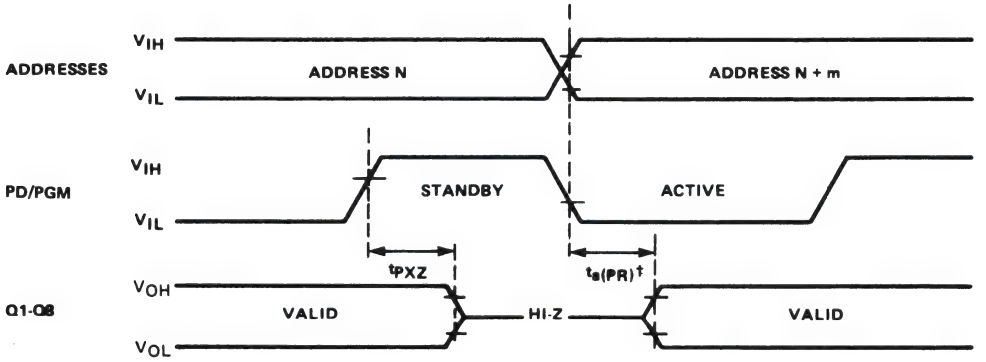
NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming. All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

5. Common test conditions apply for t_{PXZ} except during programming. For $t_{a(A)}$, $t_{a(\overline{CS})}$, and t_{PXZ}, PD/PGM = $\overline{CS}$ = V_{IL}.

read cycle timing



standby mode



NOTE: $\overline{CS}$ must be in low state during Active Mode, "Don't Care" otherwise.
†$t_{a(PR)}$ referenced to PD/PGM or the address, whichever occurs last.

All timing reference points in this data sheet (inputs and outputs) are 90% points.

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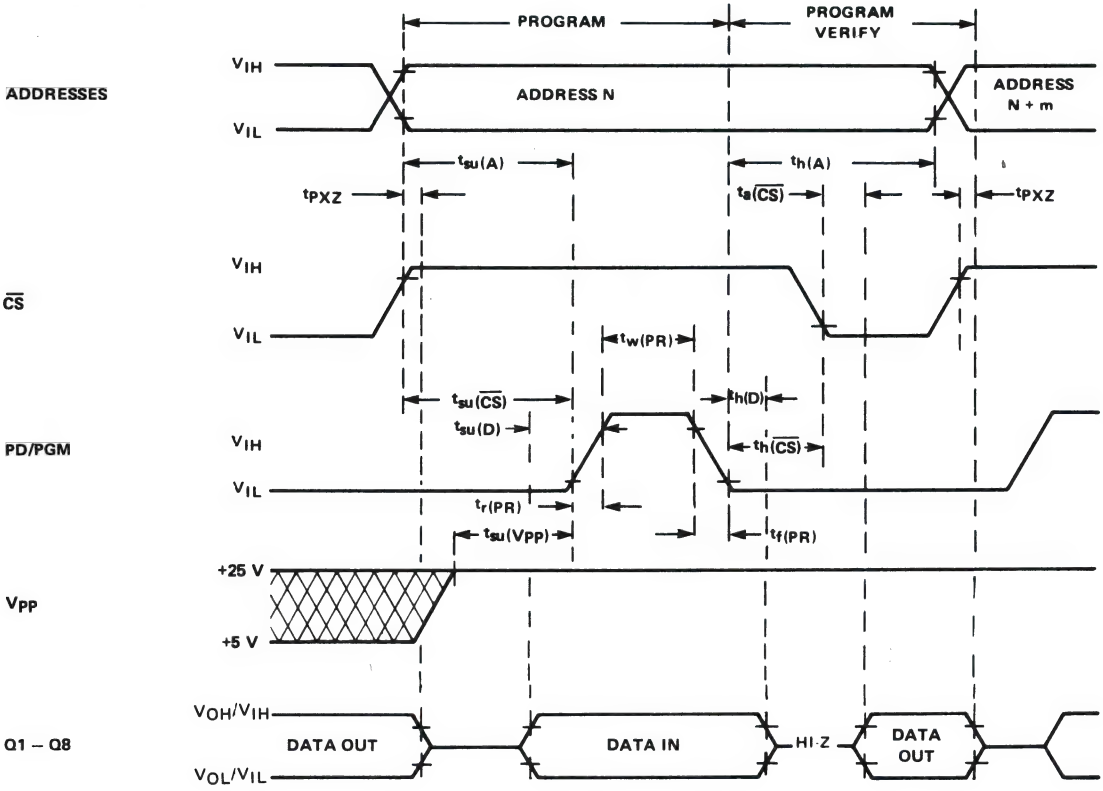
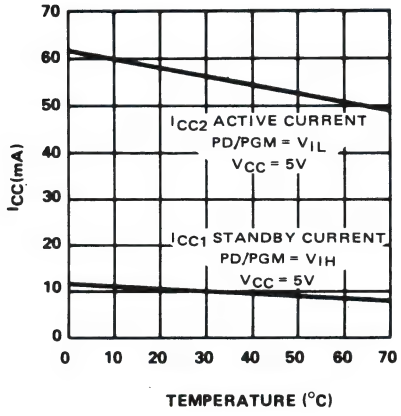
program cycle timing

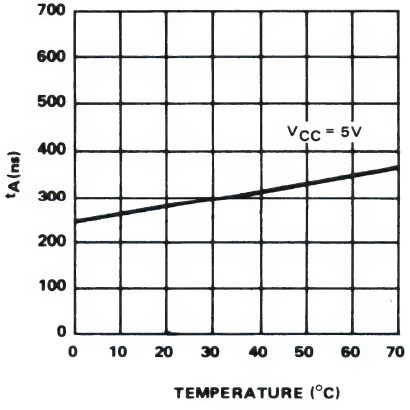


typical device characteristics (read mode)

TMS 2516
TMS 2516-35
I_{CC} CURRENT
vs
TEMPERATURE



TMS 2516
TMS 2516-35
ACCESS TIME
vs
TEMPERATURE



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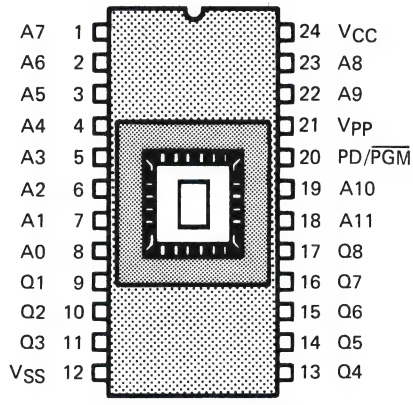
TMS 2532 JL AND TMS 25L32 JL
32,768-BIT ERASABLE
PROGRAMMABLE READ-ONLY MEMORY

DECEMBER 1979

- Organization . . . 4K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- JEDEC Standard Pinout
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- 40% Lower Power
  TMS 25L32 . . . 500 mW Max Active
  TMS 2532 . . . 840 mW Max Active
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A(N)	Address inputs
PD/$\overline{PGM}$	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2532 JL and TMS 25L32 JL are 32,768-bit, ultraviolet-light-erasable, electrically programmable read-only memories. These devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 2532 and TMS 25L32 are plug-in compatible with the TMS 4732 32K ROM. The devices are offered in a dual-in-line ceramic package (JL suffix) rated for operation from 0°C to 70°C.

Since these EPROMs operate from a single +5 V supply (in the read mode), they are ideal for use in microprocessor systems. One other (+25 V) supply is needed for programming but all programming signals are TTL level, requiring a single 50-ms pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random. Total programming time for all bits is 200 seconds.

operation

FUNCTION (PINS)	MODE				
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming
PD/$\overline{PGM}$ (20)	V_{IL}	V_{IH}	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH}
V_{PP} (21)	+5 V	+5 V	+5 V	+25 V	+25 V
V_{CC} (24)	+5 V	+5 V	+5 V	+5 V	+5 V
Q (9 to 11, 13 to 17)	Q	HI-Z	HI-Z	D	HI-Z

read/output disable

When the outputs of two or more TMS 2532's and/or TMS 25L32's are connected on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. The device whose output is to be read should have a low-level TTL signal applied to the PD/$\overline{PGM}$ pin. All other devices in the circuit should have their outputs disabled by applying a high-level signal to this pin. Output data is accessed at pins Q1 through Q8. Data can be accessed in 450 ns = $t_{a(A)}$.

power down

Active power dissipation can be cut by over 70% by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2532 or TMS 25L32 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light having a wavelength of 253.7 nm (2537 angstroms). The recommended minimum exposure dose (UV intensity times exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state (assuming high-level output corresponds to logic "1").

start programming

After erasure (all bits in logic "1" state), logic "0's" are programmed into the desired locations. A "0" can be erased only by ultraviolet light. The programming mode is achieved when V_{PP} is 25 V. Data is presented in parallel (8 bits) on pins Q1 through Q8. Once addresses and data are stable, a 50-millisecond TTL low-level pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55-milliseconds. Locations can be programmed in any order. Several TMS 2532's and/or TMS 25L32's can be programmed simultaneously when the devices are connected in parallel.

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inhibit programming

When two or more devices are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2532's and/or TMS 25L32's not intended to be programmed should have a high level applied to PD/$\overline{\text{PGM}}$.

program verification

The TMS 2532 and TMS 25L32 program verification is simply the read operation, which can be performed as soon as V_{PP} returns to +5 V ending the program cycle.

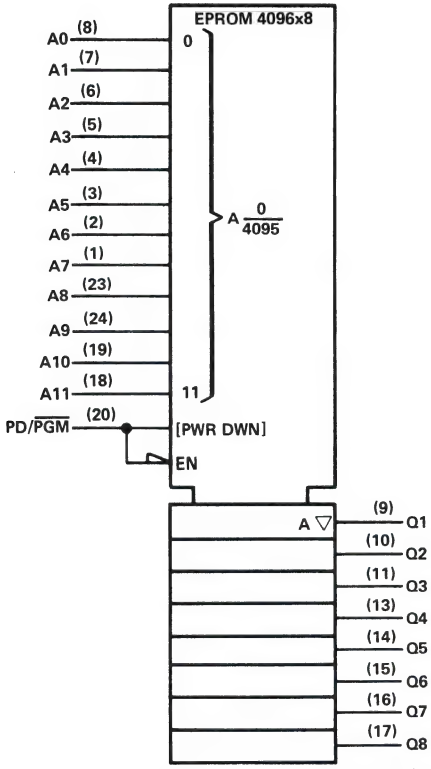
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most negative supply voltage, V_{SS} (substrate).

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	TMS 2532			TMS 25L32			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}			V_{CC}		V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH}	2.2		V_{CC}+1	2		V_{CC}+1	V
Low-level input voltage, V_{IL}	0.1		0.65	–0.1		0.8	V
Read cycle time, $t_{c(rd)}$	450			450			ns
Operating free-air temperature, T_A	0		70	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} is applied.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be $I_{CC} + I_{PP}$. During programming, V_{PP} must be maintained at 25 V (± 1V).

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS 2532			TMS 25L32			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage*	I_{OH} = –400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage*	I_{OL} = 2.1 mA			0.45			0.45	V
I_I	Input current (leakage)	V_I = 5.25 V			10			10	μA
I_O	Output current (leakage)	V_O = 5.25 V			10			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V, PD/$\overline{PGM}$ = V_{IL}			12			12	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		10	25		10	25	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160		65	95	mA

* AC and DC measurements are made at 10% and 90% points using a 50% pattern.

capacitance over recommended supply voltage and operating free-air temperature ranges, f = 1 MHz‡

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† Typical values are T_A = 25°C and nominal voltages.
‡ Capacitance measurements are made on a sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	TMS 2532 TMS 25L32 MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF,		280	450	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$	1 Series 74 TTL load,		280	450	ns
t_{PVX}	Output not valid from address change	$t_r \leqslant 20$ ns,	0			ns
t_{PXZ}	Output disable time from PD/$\overline{PGM}$	$t_f \leqslant 20$ ns	0		100	ns

† All typical values are at T_A = 25°C and nominal voltages.

recommended timing requirements for programming T_A = 25°C (see note 4)

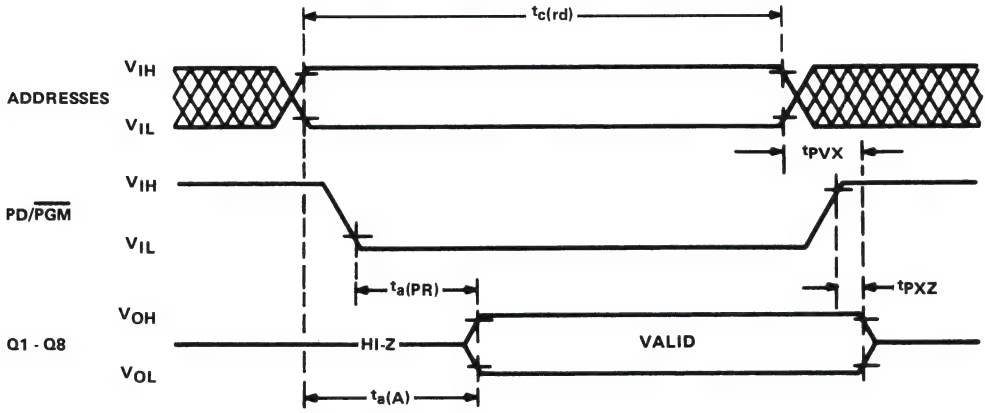
PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	0			ns

† Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming. All AC and DC measurements are made at 10% and 90% points with a 50% pattern.

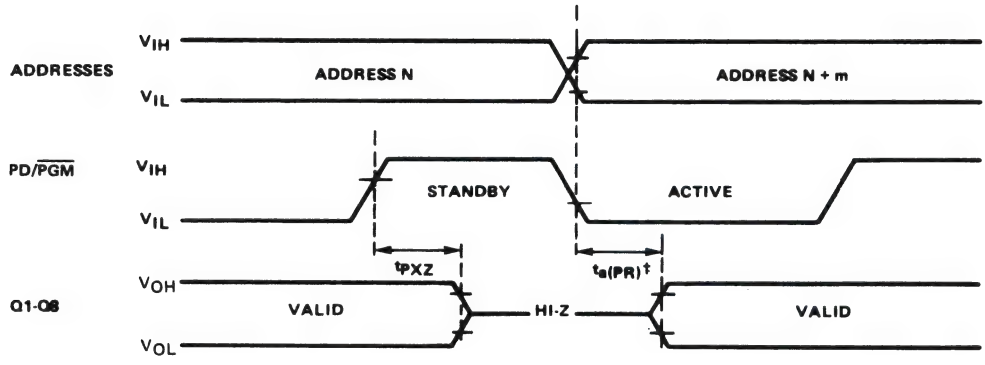
5. Common test conditions apply for t_{PXZ} except during programming. For $t_{a(A)}$ and t_{PXZ}, PD/PGM = V_{IL}.

read cycle timing



NOTE: There is no chip select pin on the TMS 2532 and TMS 25L32. The chip-select function is incorporated in the power-down mode.

standby mode



†$t_{a(PR)}$ referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.

All timing reference points in this data sheet (inputs and outputs) are 90% points.

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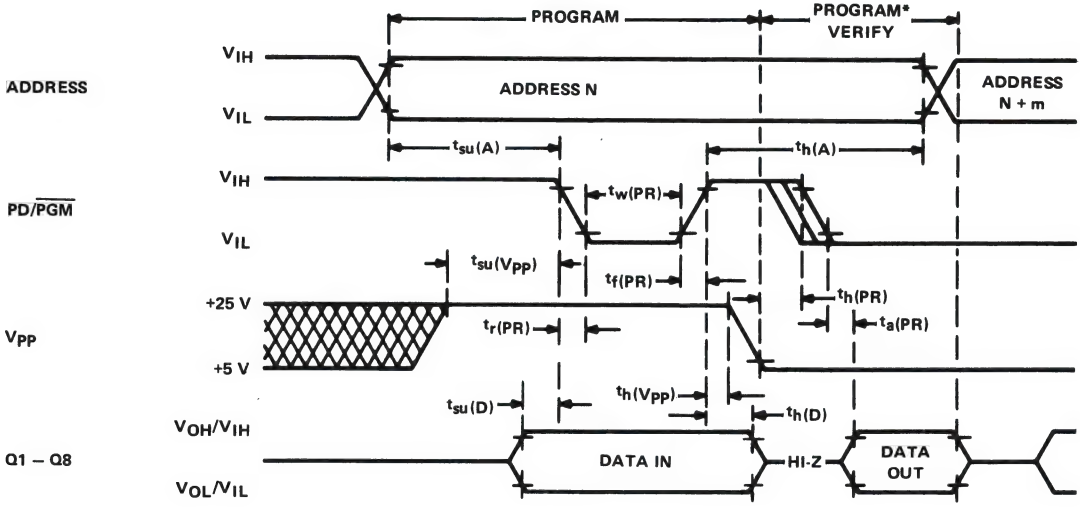
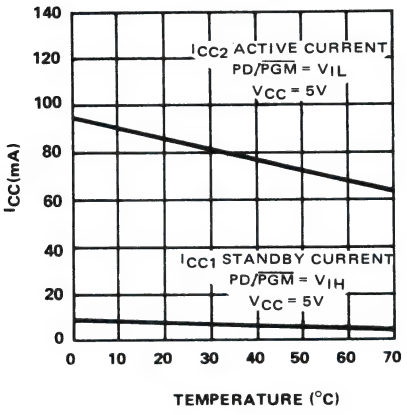
program cycle timing



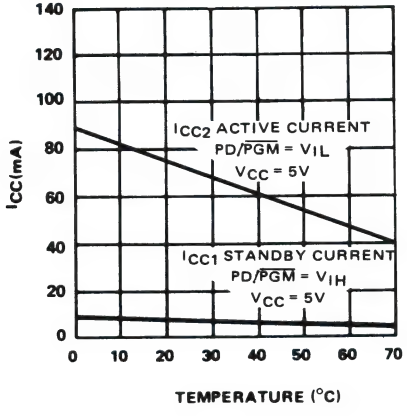
*Program verify equivalent to read mode.

typical device characteristics (read mode)

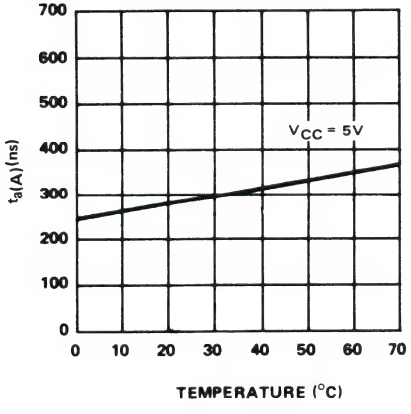
TMS 2532
I_{CC} CURRENT
vs.
TEMPERATURE



TMS 25L32
I_{CC} CURRENT
vs.
TEMPERATURE



TMS 2532
TMS 25L32
ACCESS TIME
vs
TEMPERATURE



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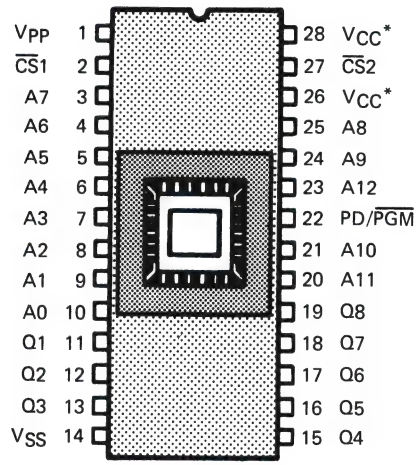
TMS 2564 JL
65,536-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

DECEMBER 1979

- Organization . . . 8K X 8
- Single +5 V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Guaranteed DC Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required
- Low Power Dissipation:

  Active . . . 400 mW Typical
  Standby . . . 50 mW Typical

TMS 2564
28-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



* Connected internally, V_{CC} need be supplied to only one of these two pins.

PIN NOMENCLATURE	
A(N)	Address inputs
$\overline{CS}$(N)	Chip Selects
PD/PGM	Power Down/Program
Q(N)	Input/Output
V_{CC}	+5 V Power Supply
V_{PP}	+25 V Power Supply
V_{SS}	0 V Ground

description

The TMS 2564 JL is a 65,536-bit, ultraviolet-light-erasable, electrically programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high-speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for connecting multiple devices to a common bus. The TMS 2564 is offered in a dual-in-line ceramic package (JL suffix) rated for operation from 0°C to 70°C.

Since this EPROM operates from a single +5 V supply (in the read mode), it is ideal for use in microprocessor systems. One other supply (+25 V) is needed for programming. Programming requires a single TTL level pulse per location. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed singly, in blocks, or at random.

The TMS 2564 is compatible with other 5-volt ROMs and EPROMs, even those in a 24-pin package.

operation

FUNCTION (PINS)	MODE				
	Read	Output Disable	Power Down	Start Programming	Inhibit Programming
PD/$\overline{PGM}$ (22)	V_{IL}	V_{IH} or Don't Care or Don't Care	V_{IH}	Pulsed V_{IH} to V_{IL}	V_{IH} or Don't Care or Don't Care
$\overline{CS}$1 (21)	V_{IL}	Don't Care or V_{IH} or Don't Care	Don't Care	V_{IL}	Don't Care or V_{IH} or Don't Care
$\overline{CS}$2 (27)	V_{IL}	Don't Care or Don't Care or V_{IH}	Don't Care	V_{IL}	Don't Care or Don't Care or V_{IH}
V_{PP} (1)	+5 V	+5 V	+5 V	+25 V	+25 V
V_{CC}* (26/28)	+5 V	+5 V	+5 V	+5 V	+5 V
Q (11 to 13, 15 to 19)	Q	HI-Z	HI-Z	D	HI-Z

* Do not use the internal jumper of 26-28 to conduct PC board currents.

read/output disable

When the outputs of two or more TMS 2564's are commoned on the same bus, the output of any particular device in the circuit can be read with no interference from the competing outputs of the other devices. To read the output of the TMS 2564, the low-level signal is applied to the PD/$\overline{PGM}$ and $\overline{CS}$ pins. All other devices in the circuit should have their outputs disabled by applying a high-level signal to one of these pins. Output data is accessed at pins Q1 to Q8. Data can be access in 450 ns = $t_{a(A)}$.

power down

Active power dissipation can be cut by one of over 80% by applying a high TTL signal to the PD/$\overline{PGM}$ pin. In this mode all outputs are in a high-impedance state.

erasure

Before programming, the TMS 2564 is erased by exposing the chip through the transparent lid to high intensity ultraviolet (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. A typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in about 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the high state.

start programming

After erasure (all bits in logic high state), logic "0's" are programmed into the desired locations. A low can be erased only by ultraviolet light. The programming mode is achieved when Vpp is 25 V. Data is presented in parallel (8 bits) on pins Q1 to Q8. Once addresses and data are stable, a 50 millisecond low TTL pulse should be applied to the $\overline{PGM}$ pin at each address location to be programmed. Maximum pulse width is 55 milliseconds. Locations can be programmed in any order. More than one TMS 2564 can be programmed when the devices are connected in parallel. During programming both chip select signals should be held low unless program inhibit is desired.

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inhibit programming

When two or more TMS 2564's are connected in parallel, data can be programmed into all devices or only chosen devices. TMS 2564's not intended to be programmed should have a high level applied to PD/$\overline{PGM}$ or $\overline{CS1}$ or $\overline{CS2}$.

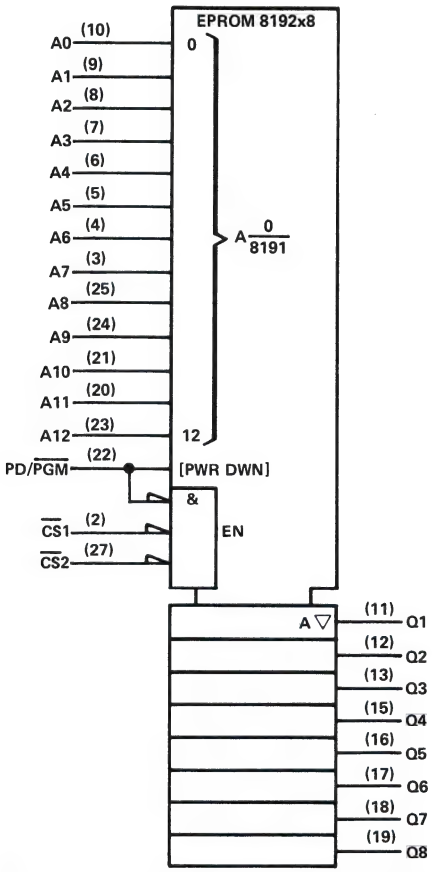
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 6 V
Supply voltage, V_{PP} (see Note 1)	−0.3 to 28 V
All input voltages (see Note 1)	−0.3 to 6 V
Output voltage (operating with respect to V_{SS})	−0.3 to 6 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{SS} (substrate).

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC} (see Note 2)	4.75	5	5.25	V
Supply voltage, V_{PP} (see Note 3)		V_{CC}		V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2.2		V_{CC}+1	V
Low-level input voltage, V_{IL}	−0.1††		0.65	V
Read cycle time, $t_{c(rd)}$	450			ns
Operating free-air temperature, T_A	0		70	°C

NOTES: 2. V_{CC} must be applied before or at the same time as V_{PP} and removed after or at the same time as V_{PP}. The device must not be inserted into or removed from the board when V_{PP} or V_{CC} is applied so that the device is not damaged.

3. V_{PP} can be connected to V_{CC} directly (except in the program mode). V_{CC} supply current in this case would be I_{CC} + I_{PP}. During programming, V_{PP} must be maintained at 25 V (± 1V).

†† The algebraic convention where the more negative limit is designated as minimum is used in this data sheet for logic voltage levels and time intervals.

electrical characteristics over full ranges of recommended operating conditions

PARAMETER		TEST CONDITIONS	TMS 2564 MIN	TMS 2564 TYP†	TMS 2564 MAX	UNIT
V_{OH}	High-level output voltage*	I_{OH} = −400 μA	2.4			V
V_{OL}	Low-level output voltage*	I_{OL} = 2.1 mA			0.45	V
I_I	Input current (leakage)	V_I = 5.25 V			10	μA
I_O	Output current (leakage)	V_O = 5.25 V			10	μA
I_{PP1}	V_{PP} supply current	V_{PP} = 5.25 V PD/$\overline{PGM}$ = V_{IL}			12	mA
I_{PP2}	V_{PP} supply current (during program pulse)	PD/$\overline{PGM}$ = V_{IL}			30	mA
I_{CC1}	V_{CC} supply current (standby)	PD/$\overline{PGM}$ = V_{IH}		10	25	mA
I_{CC2}	V_{CC} supply current (active)	PD/$\overline{PGM}$ = V_{IL}		80	160	mA

† Typical values are at T_A = 25°C and nominal voltages.

* AC and DC tests are made at 10% and 90% points using a 50% pattern.

capacitance over recommended supply voltage and operating free-air temperature range f = 1 MHz*

PARAMETER		TEST CONDITIONS	TYP†	MAX	UNIT
C_i	Input capacitance	V_I = 0 V, f = 1 MHz	4	6	pF
C_o	Output capacitance	V_O = 0 V, f = 1 MHz	8	12	pF

† All typical values are T_A = 25°C and nominal voltage.

* This parameter is tested on sample basis only.

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switching characteristics over full ranges of recommended operating conditions (see note 4)

PARAMETER		TEST CONDITIONS (SEE NOTES 4 AND 5)	MIN	TYP†	MAX	UNIT
$t_{a(A)}$	Access time from address	C_L = 100 pF, 1 Series 74 TTL load, $t_r \leq 20$ ns, $t_f \leq 20$ ns		280	450	ns
$t_{a(S)}$	Access time from $\overline{CS1}$ and $\overline{CS2}$ (whichever occurs last)				120	ns
$t_{a(PR)}$	Access time from PD/$\overline{PGM}$			280	450	ns
t_{PVX}	Output not valid from address change		0			ns
t_{PXZ}	Output disable time from chip deselect during read only (whichever occurs last)		0		100	ns
t_{PXZ}	Output disable time from PD/$\overline{PGM}$ during standby		0		100	ns

† All typical values are at T_A = 25°C and nominal voltages.

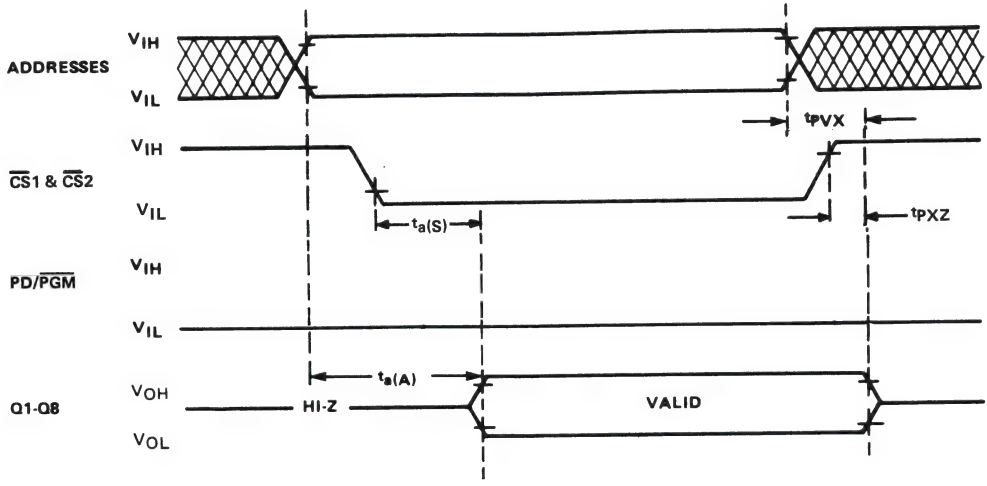
recommended timing requirements for programming T_A = 25°C (see note 4)

PARAMETER		MIN	TYP†	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	45	50	55	ms
$t_{r(PR)}$	Rise time, program pulse	5			ns
$t_{f(PR)}$	Fall time, program pulse	5			ns
$t_{su(A)}$	Address setup time	2			μs
$t_{su(D)}$	Data setup time	2			μs
$t_{su(VPP)}$	Setup time from V_{PP}	0			ns
$t_{h(A)}$	Address hold time	2			μs
$t_{h(D)}$	Data hold time	2			μs
$t_{h(PR)}$	Program pulse hold time	0			ns
$t_{h(VPP)}$	V_{PP} hold time	0			ns

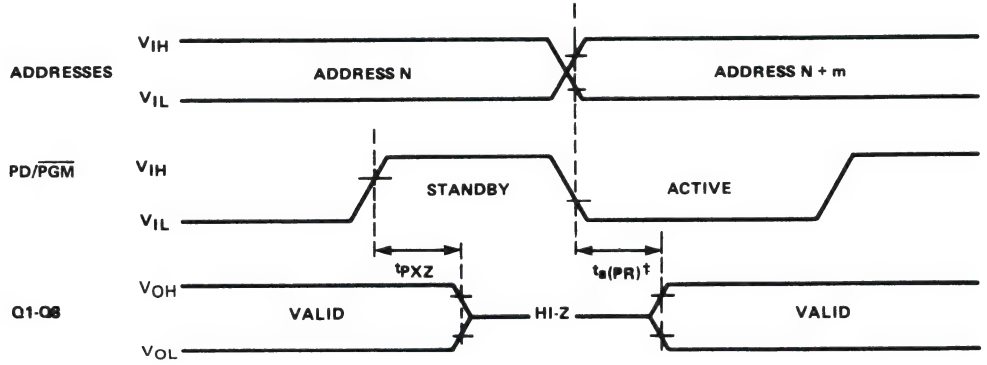
† Typical values are at nominal voltages.

NOTES: 4. For all switching characteristics and timing measurements, input pulse levels are 0.65 V to 2.2 V and V_{PP} = 25 V ± 1 V during programming. AC and DC timing measurements are made at 90% points using a 50% pattern.
5. Common test conditions apply for t_{PXZ} except during programming. For $t_{a(A)}$, $t_{a(S)}$, and t_{PXZ}, PD/PGM = V_{IL}.

read cycle timing



standby mode



NOTE: † $t_{a(PR)}$ referenced to PD/$\overline{PGM}$ or the address, whichever occurs last.
$\overline{CS1}$ and $\overline{CS2}$ in Don't Care State in Standby Mode.

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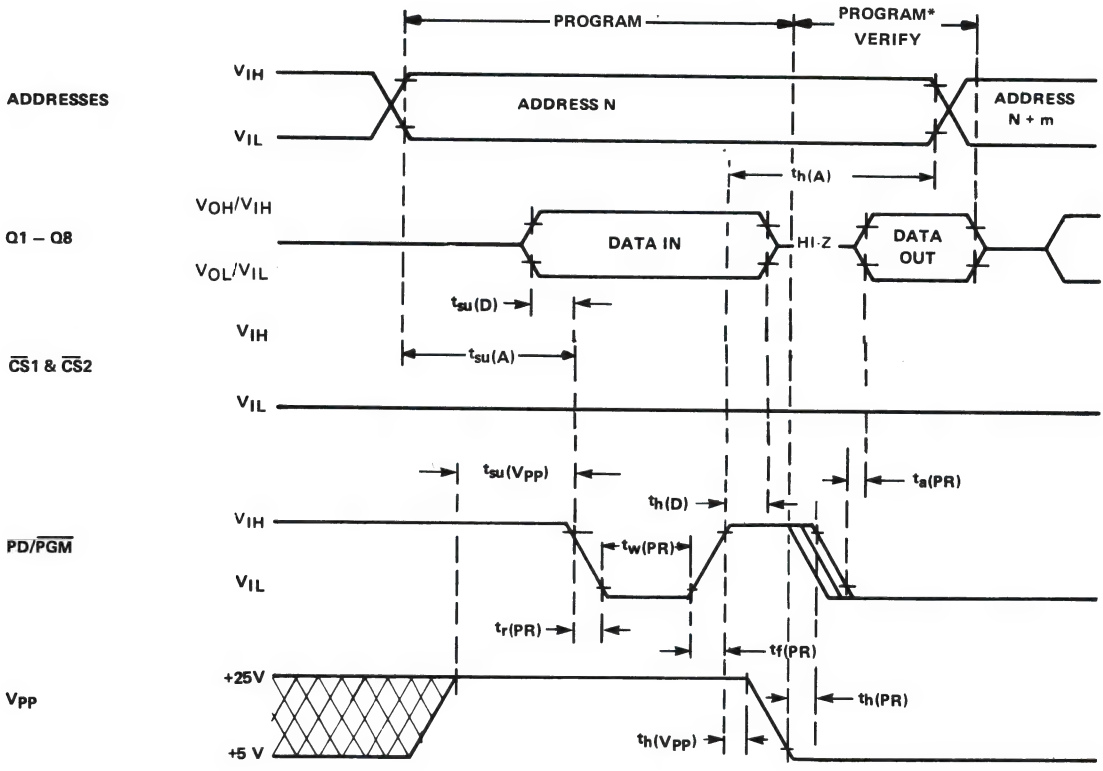
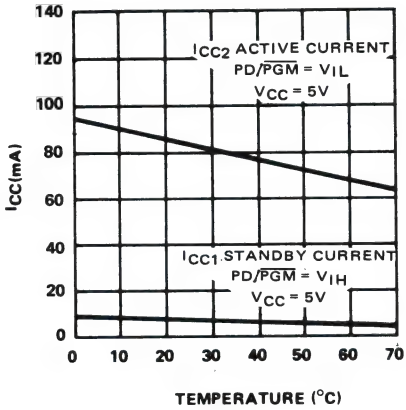
program cycle timing



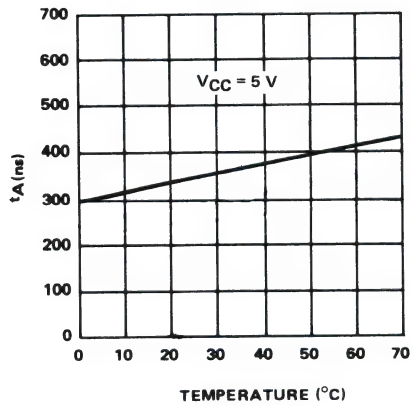
* Equivalent to read mode.

typical device characteristics (read mode)

TMS 2564
I_{CC} CURRENT
vs
TEMPERATURE



TMS 2564
ACCESS TIME
vs
TEMPERATURE



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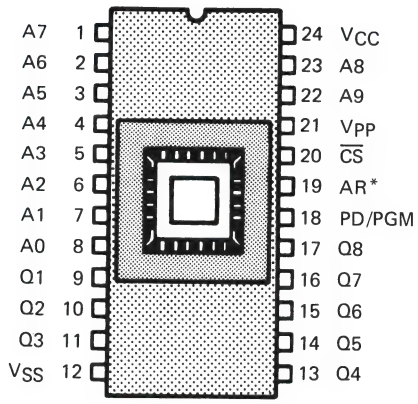
TMS 2758 JL
8,192-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

DECEMBER 1979

- 1K X 8 Organization
- Single +5-V Power Supply
- Pin Compatible with Existing ROMs and EPROMs (8K, 16K, 32K, and 64K)
- Pin-Compatible With I2758
- All Inputs/Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Max Access/Min Cycle Time . . . 450 ns
- 8-Bit Output for Use in Microprocessor-Based Systems
- N-Channel Silicon-Gate Technology
- 3-State Output Buffers
- Low Power Dissipation
  - Active . . . 285 mW Typical
  - Standby . . . 50 mW Typical
- Guaranteed dc Noise Immunity with Standard TTL Loads
- No Pull-Up Resistors Required

TMS 2758
24-PIN CERAMIC
DUAL-IN-LINE PACKAGE
(TOP VIEW)



* AR tied to V_{IL} if TMS 2758-JL0
V_{IH} if TMS 2758-JL1

PIN NOMENCLATURE	
A0 thru A7	Address inputs
AR	Array Select
PD/PGM	Power Down/Program
Q1 thru Q8	Input/Output
$\overline{CS}$	Chip Select
V_{CC}	Operating Power Supply
V_{PP}	Programming Power Supply
V_{SS}	0 V Ground

description

The TMS 2758 is an 8,192-bit, ultraviolet-light-erasable, electrically programmable read-only memory. This device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by series 74 TTL circuits without the use of external pull-up resistors, and each output can drive one Series 74 TTL circuit without external resistors. The data outputs are three-state for wired-OR connection of multiple devices on a common bus. The TMS 2758 is pin-compatible with the TMS 2516 16K EPROM.

Since this EPROM operates from a single +5-V supply in the read mode, it is ideal for use in microprocessor systems. One other supply (+25 V) is needed for programming, but all programming signals are TTL levels and require a single 50-millisecond pulse. For programming outside of the system, existing EPROM programmers can be used. Locations may be programmed sequentially, in blocks, or at random. Total required programming time for all bits for the TMS 2758 is 50 seconds.

The TMS 2758 is offered in dual-in-line cerpak (JL suffix) package rated for operation from 0°C to 70°C.

Complete information may be obtained from your local TI Sales Office or authorized distributor listed near the front of this data book.

TMS 2708 JL, TMS 2708-35 JL, TMS 27L08 JL
1024-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORIES

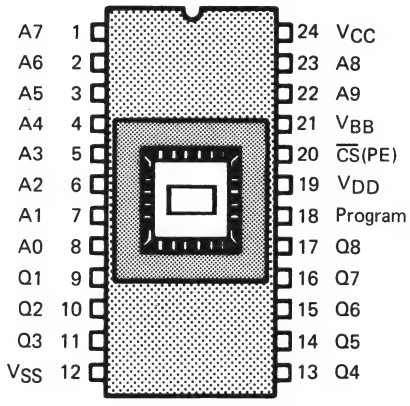
DECEMBER 1979

- 1024 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Performance Ranges

	Max Access	Min Cycle
TMS 2708-35	350 ns	350 ns
TMS 2708	450 ns	450 ns
TMS 27L08	450 ns	450 ns

- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power on TMS 27L08 . . . 245 mW (Typ)
- 10% Power Supply Tolerance (TMS 27L08 Only)
- Plug-Compatible Pin-Outs Allowing Interchangeability/Upgrade to 16K With Minimum Board Change

24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 2708, TMS 2708-35, and TMS 27L08 JL are ultra-violet light-erasable, electrically programmable read only memories. They have 8,192 bits organized as 1024 words of 8-bit length. The devices are fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 TTL circuits without the use of external pull-up resistors. Each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS 27L08 guarantees 200 mV dc noise immunity in the high state and 250 mV in the low state. The data outputs for the TMS 2708, TMS 2708-35 and TMS 27L08 are three-state for OR-tying multiple devices on a common bus.

These EPROMs are designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. They are supplied in a 24-pin dual-in-line ceramic cerdip (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers. They are designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A9)

The address-valid interval determines the device cycle time. The 10-bit positive-logic address is decoded on-chip to select one of the 1024 words of 8-bit length in the memory array. A0 is the least-significant bit and A9 is the most-significant bit of the word address.

chip select, program enable [$\overline{CS}$ (PE)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

program

The program pin must be held below V_{CC} in the read mode.

operation (program mode)

erase

Before programming, the TMS 2708, TMS 2708-35, or TMS 27L08 is erased by exposing the chip through the transparent lid to high-intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity X exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a mimimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25°C) only.

to start programming (see program cycle timing diagram)

First bring the $\overline{CS}$ (PE) pin to +12 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +25 V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with N x $t_{W(PR)} \geqslant 100$ ms. Thus, if $t_{W(PR)} = 1$ ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable [$\overline{CS}$ (PE)] is brought to V_{IL} which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to V_{IL}.

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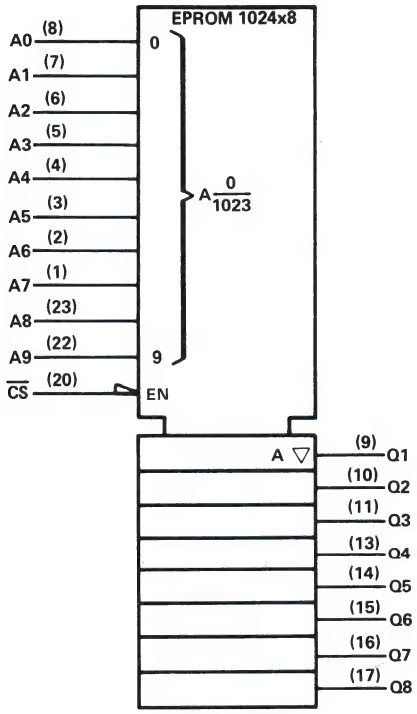
absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 15 V
All input voltage (except program) (see Note 1)	−0.3 to 20 V
Program Input (see Note 1)	−0.3 to 35 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

logic symbol†



†This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	TMS 2708-35, TMS 2708			TMS 27L08			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{BB}	−4.75	−5	−5.25	−4.5	−5	−5.5	V
Supply voltage, V_{CC}	4.75	5	5.25	4.5	5	5.5	V
Supply voltage, V_{DD}	11.4	12	12.6	10.8	12	13.2	V
Supply voltage, V_{SS}		0			0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		V_{CC}+1	2.2		V_{CC}+1	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	10.8	12	13.2	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V_{SS}		0.65	V
Low-level program input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ −25 V	V_{SS}		1	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40			40	mA
Low-level program pusle input current (source), $I_{IL(PR)}$			3			3	mA
Operating free-air temperature, T_A	0		70	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS 2708-35, TMS 2708			TMS 27L08			UNITS
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{OH}	High-level output voltage	I_{OH} = −100 μA	3.7			3.7			V
		I_{OH} = −1 mA	2.4			2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA			0.45			0.40	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V		1	10		1	10	μA
I_O	Output current (leakage)	$\overline{CS}$(PE) = 5 V		1	10		1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high		30	45		9	18	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$(PE) = 5 V		6	10		.9	6	mA
I_{DD}	Supply current from V_{DD}	For I_{DD} MAX, T_A = 0°C (worst case)		50	65		20	34	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C			800			350	mW
		T_A = 0°C $\overline{CS}$ = 0 V					245	475	
		T_A = 0°C $\overline{CS}$ = +5 V					290	580	

†All typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

PARAMETER		TYP†	MAX	UNIT
C_i	Input capacitance	4	6	pF
C_o	Output capacitance	8	12	pF

†All typical values are at T_A = 25°C and nominal voltages.

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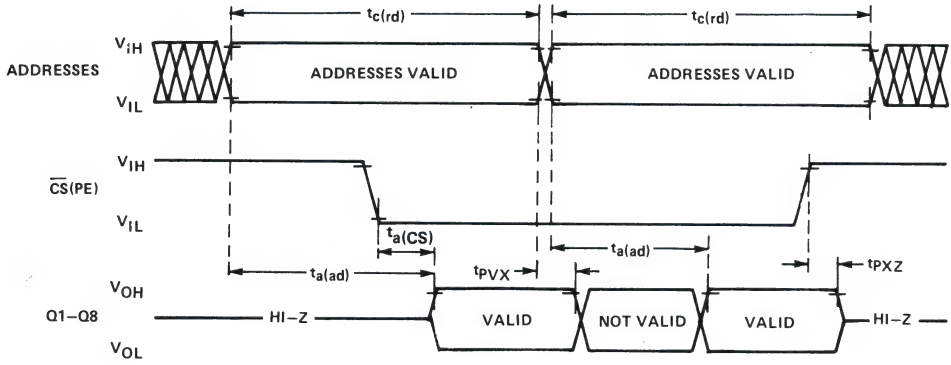
switching characteristics over recommended supply voltage range and operating free-air temperature range

PARAMETER		TEST CONDITIONS	TMS 2708-35		TMS 2708 TMS 27L08		UNIT
			MIN	MAX	MIN	MAX	
$t_{a(ad)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns		350		450	ns
$t_{a(CS)}$	Access time from $\overline{CS}$			120		120	ns
t_{PVX}	Output invalid from address change		0		0		ns
t_{PXZ}	Output disable time		0	120	0	120	ns
$t_{c(rd)}$	Read Cycle time		350		450		ns

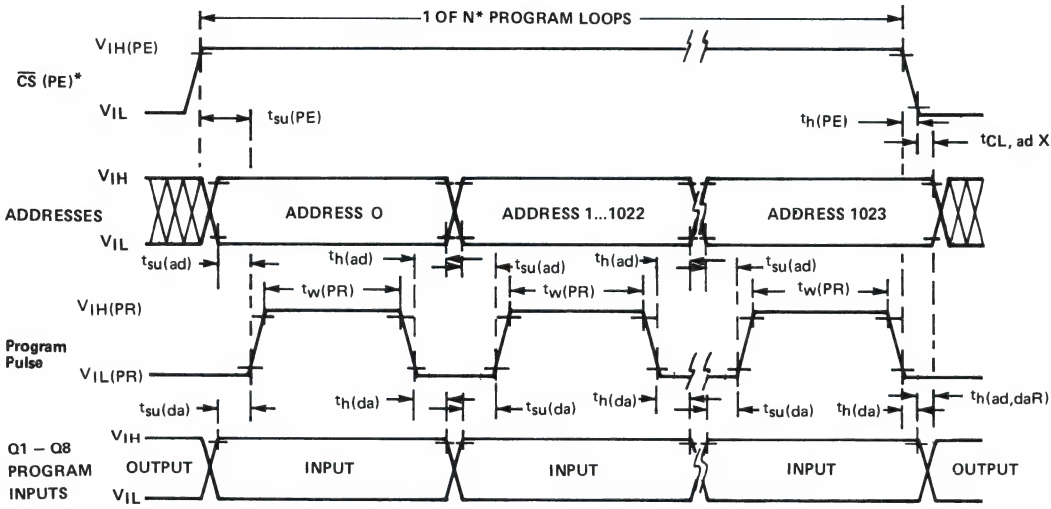
T_A = 25°C program characteristics over recommended supply voltage range

PARAMETER		MIN	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	50	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,da\ R)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, $\overline{CS}$(PE) low to address change	0		ns

read cycle timing



program cycle timing



*$\overline{CS}$ (PE) is at +12 V through N program loops where N $\geqslant$ 100 ms/tw (PR).

NOTE: Q1-Q8 outputs are invalid up to 10 μsec after programming [$\overline{CS}$(PE) goes low].

All timing reference points in this data sheet (inputs and outputs) are 90% points.

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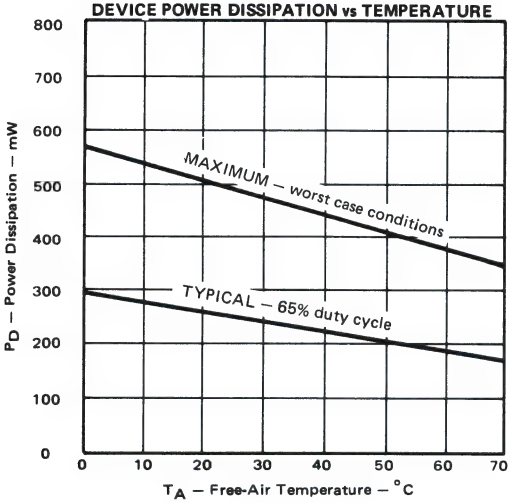
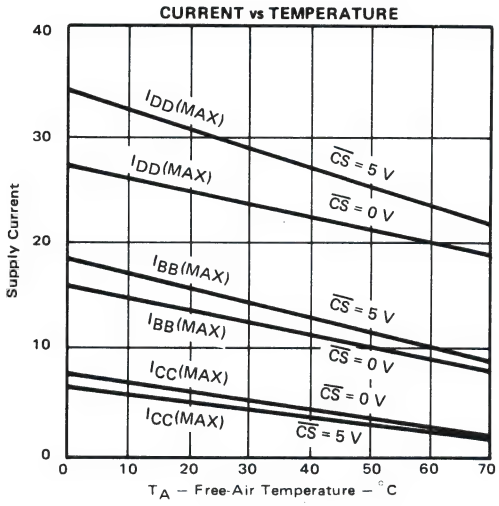
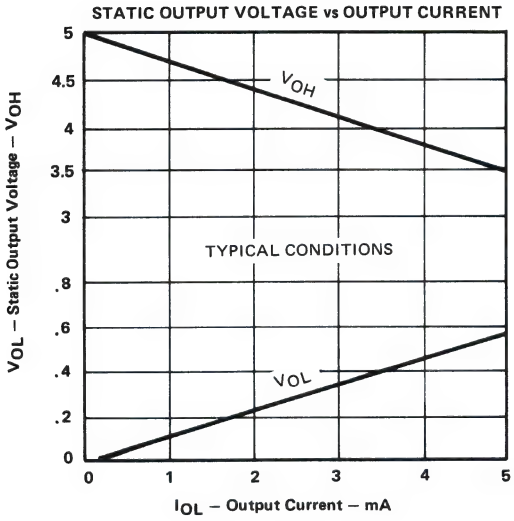
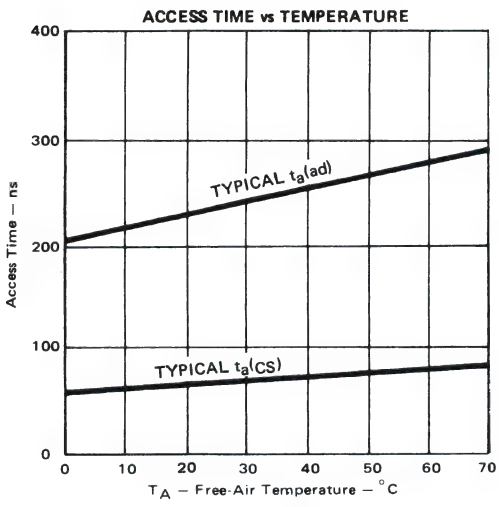
TYPICAL TMS 27L08 CHARACTERISTICS







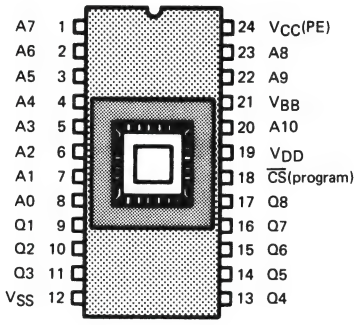


TMS 2716 JL
2048-WORD BY 8-BIT ERASABLE PROGRAMMABLE READ-ONLY MEMORY

DECEMBER 1979

- 2048 X 8 Organization
- All Inputs and Outputs Fully TTL Compatible
- Static Operation (No Clocks, No Refresh)
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- 3-State Outputs for OR-Ties
- N-Channel Silicon-Gate Technology
- 8-Bit Output for Use in Microprocessor-Based Systems
- Low Power . . . 315 mW (Typical)

24-PIN CERPAK
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TMS 2716JL is an ultra-violet light-erasable, electrically programmable read only memory. It has 16,384 bits organized as 2048 words of 8-bit length. The device is fabricated using N-channel silicon-gate technology for high speed and simple interface with MOS and bipolar circuits. All inputs (including program data inputs) can be driven by Series 74 circuits without the use of external pull-up resistors and each output can drive one Series 74 or 74LS TTL circuit without external resistors. The TMS 2716 guarantees 250 mV dc noise immunity in the low state. Data outputs are three-state for OR-tying multiple devices on a common bus. The TMS 2716 is plug-in compatible with the TMS 2708 and the TMS 27L08. Pin compatible mask programmed ROMs are available for large volume requirements.

This EPROM is designed for high-density fixed-memory applications where fast turn arounds and/or program changes are required. It is supplied in a 24-pin dual-in-line cerpak (JL suffix) package designed for insertion in mounting-hole rows on 600-mil (15.2 mm) centers. It is designed for operation from 0°C to 70°C.

operation (read mode)

address (A0-A10)

The address-valid interval determines the device cycle time. The 11-bit positive-logic address is decoded on-chip to select one of 2048 words of 8-bit length in the memory array. A0 is the least-significant bit and A10 most-significant bit of the word address.

chip select, program [CS (Program)]

When the chip select is low, all eight outputs are enabled and the eight-bit addressed word can be read. When the chip select is high, all eight outputs are in a high-impedance state.

program

In the program mode, the chip select feature does not function as pin 18 inputs only the program pulse. The program mode is selected by the V_{CC}(PE) pin. Either 0 V or +12 V on this pin will cause the TMS 2716 to assume program cycle.

data out (Q1-Q8)

The chip must be selected before the eight-bit output word can be read. Data will remain valid until the address is changed or the chip is deselected. When deselected, the three-state outputs are in a high-impedance state. The outputs will drive TTL circuits without external components.

operation (program mode)

erase

Before programming, the TMS 2716 is erased by exposing the chip through the transparent lid to high intensity ultraviolet light (wavelength 2537 angstroms). The recommended minimum exposure dose (= UV intensity × exposure time) is fifteen watt-seconds per square centimeter. Thus, a typical 12 milliwatt per square centimeter, filterless UV lamp will erase the device in a minimum of 21 minutes. The lamp should be located about 2.5 centimeters above the chip during erasure. After erasure, all bits are in the "1" state.

programming

Programming consists of successively depositing a small amount of charge to a selected memory cell that is to be changed from the erased high state to the low state. A low can be changed to a high only by erasure. Programming is normally accomplished on a PROM or EPROM Programmer, an example of which is TI's Universal PROM Programming Module in conjunction with the 990 prototyping system. Programming must be done at room temperature (25°C) only.

to start programming (see program cycle timing diagram)

First bring the $V_{CC}(PE)$ pin to +12 V or 0 V to disable the outputs and convert them to inputs. This pin is held high for the duration of the programming sequence. The first word to be programmed is addressed (it is customary to begin with the "0" address) and the data to be stored is placed on the Q1-Q8 program inputs. Then a +26V program pulse is applied to the program pin. After 0.1 to 1.0 milliseconds the program pin is brought back to 0 V. After at least one microsecond the word address is sequentially changed to the next location, the new data is set up and the program pulse is applied.

Programming continues in this manner until all words have been programmed. This constitutes one of N program loops. The entire sequence is then repeated N times with $N \times t_{W(PR)} \geq 100$ ms. Thus, if $t_{W(PR)} =$ 1 ms; then N = 100, the minimum number of program loops required to program the EPROM.

to stop programming

After cycling through the N program loops, the last program pulse is brought to 0 V, then Program Enable $V_{CC}(PE)$ is brought back to ±5 volts which takes the device out of the program mode. The data supplied by the programmer must be removed before the address is changed since the program inputs are now data outputs and a change of address could cause a voltage conflict on the output buffer. Q1-Q8 outputs are invalid up to 10 microseconds after the program enable pin is brought from $V_{IH(PE)}$ to $V_{IL(PE)}$.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1)	−0.3 to 15 V
Supply voltage, V_{DD} (see Note 1)	−0.3 to 20 V
Supply voltage, V_{SS} (see Note 1)	−0.3 to 15 V
All input voltage (except program) (see Note 1)	−0.3 to 20 V
Program Input (see Note 1)	−0.3 to 35 V
Output voltage (operating, with respect to V_{SS})	−2 to 7 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 125°C

NOTE 1: Under absolute maximum ratings, voltage values are with respect to the most-negative supply voltage, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this data sheet, voltage values are with respect to V_{SS}.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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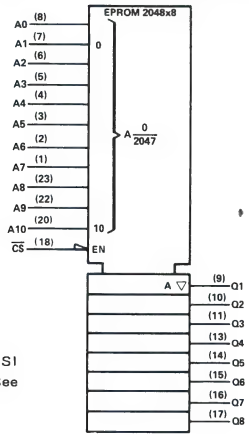
functional block diagram*



* This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEEE and IEC. See explanation on page 183.

recommended operating conditions

PARAMETER	MIN	NOM	MAX	UNIT
Supply voltage, V_{BB}	−4.75	−5	−5.25	V
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{DD}	11.4	12	12.6	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH} (except program and program enable)	2.4		V_{CC}+1	V
High-level program enable input voltage, $V_{IH(PE)}$	11.4	12	12.6	V
High-level program input voltage, $V_{IH(PR)}$	25	26	27	V
Low-level input voltage, V_{IL} (except program)	V_{SS}		0.65	V
Low-level porgram input voltage, $V_{IL(PR)}$ Note: $V_{IL(PR)}$ max ≤ $V_{IH(PR)}$ −25 V	V_{SS}		1	V
High-level program pulse input current (sink), $I_{IH(PR)}$			40	mA
Low-level program pulse input current (source), $I_{IL(PR)}$			3	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNITS
V_{OH}	High-level output voltage	I_{OH} = −100 μA		3.7			V
		I_{OH} = −1 mA		2.4			
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA				0.45	V
I_I	Input current (leakage)	V_I = 0 V to 5.25 V			1	10	μA
I_O	Output current (leakage)	$\overline{CS}$ (Program) = 5 V			1	10	μA
I_{BB}	Supply current from V_{BB}	All inputs high			10	20	mA
I_{CC}	Supply current from V_{CC}	$\overline{CS}$ (Program) = 5 V			1	8	mA
I_{DD}	Supply current from V_{DD}	For I_{DD} MAX,	T_A = 0°C (worst case)		26	45	mA
I_{PE}	Supply current from PE on V_{CC} Pin	V_{PE} = V_{DD}			2	4	mA
$P_{D(AV)}$	Power Dissipation	T_A = 70°C				540	mW
		T_A = 0°C	$\overline{CS}$ = 0 V		315	595	
		T_A = 0°C	$\overline{CS}$ = +5 V		375	720	

†All typical values are at T_A = 25°C and nominal voltages.

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz

	PARAMETER	TYP†	MAX	UNIT
C_i	Input capacitance [except CS (Program)]	4	6	pF
$C_{i(CS)}$	$\overline{CS}$ (Program) input capacitance	20	30	pF
C_o	Output cpacitance	8	12	pF

†All typical values are at T_A = 25°C and nominal voltages.

switching characteristics over recommended supply voltage range and operating free-air temperature range

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$t_{a(ad)}$	Access time from address	C_L = 100 pF 1 Series 74 TTL Load $t_{f(CS)}$, $t_{f(ad)}$ = 20 ns		450	ns
$t_{a(CS)}$	Access time from $\overline{CS}$			120	ns
t_{PVX}	Output invalid from address change		0		ns
t_{PXZ}	Output disable time		0	120	ns
$t_{c(rd)}$	Read Cycle time		450		ns

T_A = 25°C program characteristics over recommended supply voltage range

	PARAMETER	MIN	MAX	UNIT
$t_{w(PR)}$	Pulse width, program pulse	0.1	1	ms
t_T	Transition times (except program pulse)		20	ns
$t_{T(PR)}$	Transition times, program pulse	50	2000	ns
$t_{su(ad)}$	Address setup time	10		μs
$t_{su(da)}$	Data setup time	10		μs
$t_{su(PE)}$	Program enable setup time	10		μs
$t_{h(ad)}$	Address hold time	1000		ns
$t_{h(ad,da\ R)}$	Address hold time after program input data stopped	0		ns
$t_{h(da)}$	Data hold time	1000		ns
$t_{h(PE)}$	Program enable hold time	500		ns
$t_{CL,adX}$	Delay time, $\overline{CS}$ (Program) low to address change	0		ns

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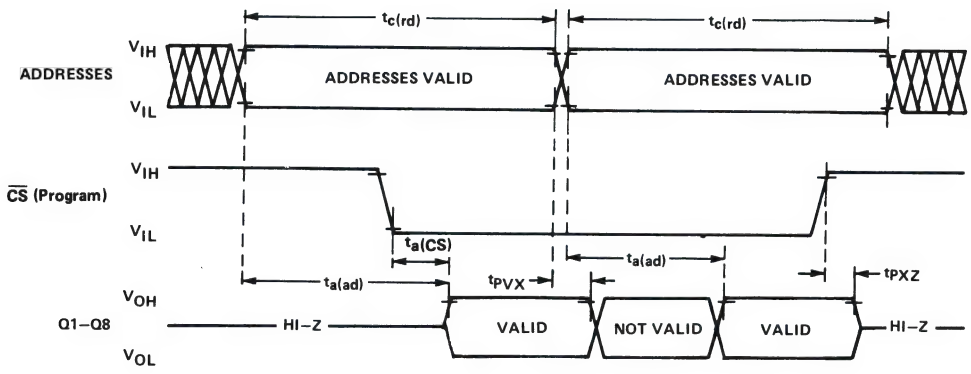
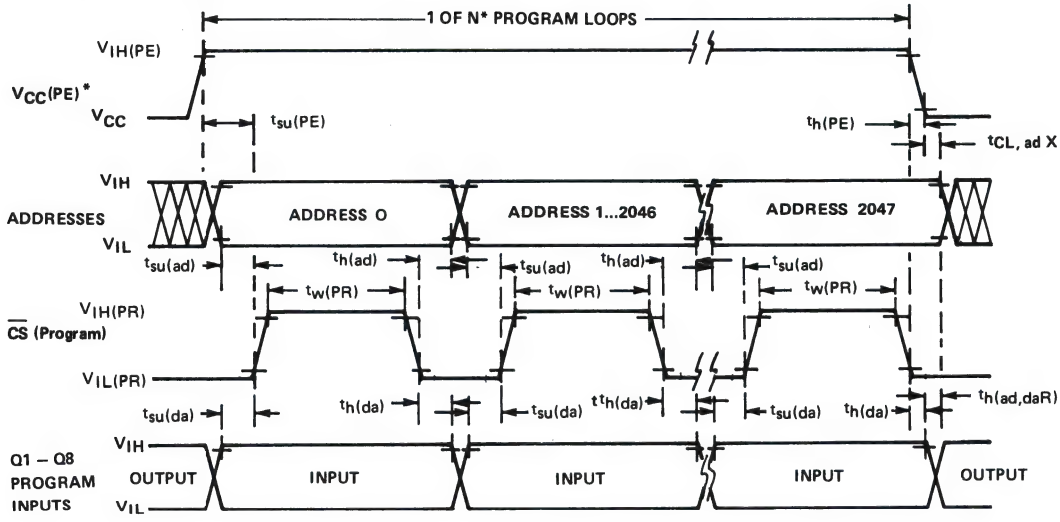
read cycle timing



program cycle timing



*V_{CC} (PE) is at 0 V or +12 V through N program loops where N ⩾ 100 ms/tw (PR).

NOTE. Q1-Q8 outputs are invalid up to 10 μsec after programing (V_{CC} (PE) goes low).

APPLICATIONS INFORMATION

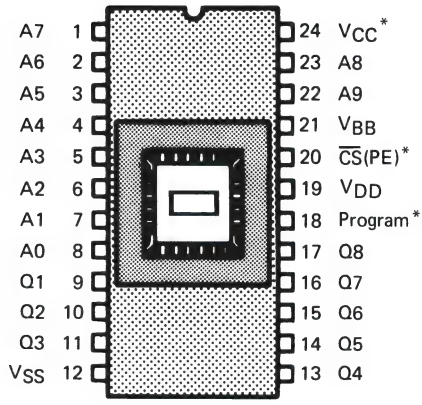
Ease of Conversion From TMS 2708 To TMS 2716

A. The TMS 2716 and TMS 2708 have compatible timing, voltage and current parameters in both modes.

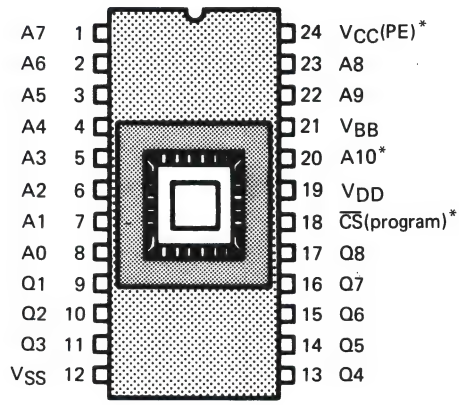
B. The TMS 2716 requires less power than the TMS 2708.

C. The pinouts are compatible. (See below.)

TMS 2708



TMS 2716



As can be seen from the above diagrams, only three pins* are modified in going from TMS 2708 to TMS 2716:

1. The additional address pin requrired for the 16K EPROM is located on pin 20 which displaces the $\overline{CS}$/PE functions on the TMS 2708.

2. Since the V_{CC} is not required during programming, the PE function shares pin 24 with V_{CC} on the TMS 2716.

3. The $\overline{CS}$ function and program function are mutually exclusive during normal read mode (and are self-actuated complementary during the program/verify mode) and share pin 18 on the TMS 2716.

The diagrams below show how these three pins are actually utilized in the read mode and in the program mode. Only pins 18, 20, and 24 need to be shown, as all other pin connections are identical.

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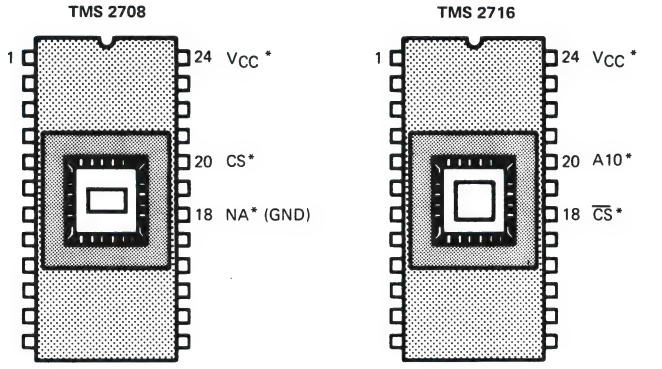
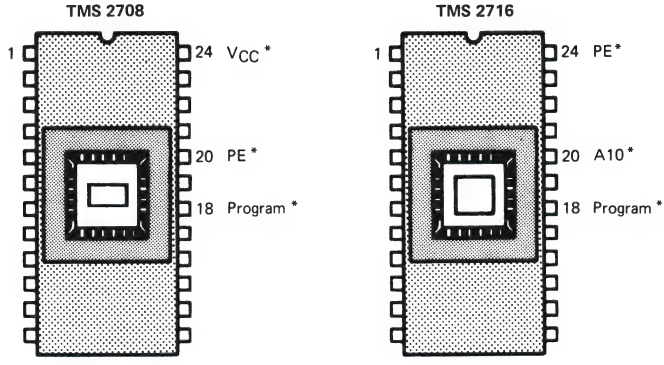
Read Mode



Program (Write) Mode



TMS 2716 — Easy Programmability On Existing 2708 Programmers

Existing EPROM Programmers — Upgrading To The TMS 2716

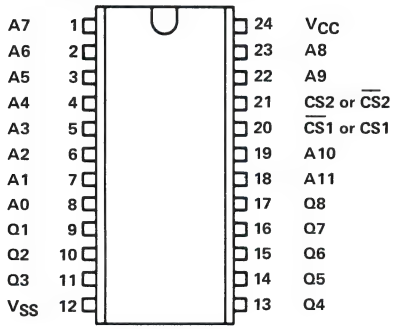
Most of the EPROM manufacturers have implemented field upgrade modifications to allow TMS 2716 programming on current EPROM programmers. This is greatly simplified because the TMS 2716 and the TMS 2708 are programmed in an identical manner. A slight modification to the socket card, an additonal 1K × 8 of RAM, and an extra address signal (A10) are all that is required. All timing and voltage parameters are identical, so the upgrade is easily accomplished. Programmer manufacturers contacted to date on the TMS 2716 include: Data I/O, PRO LOG, Texas Instruments, Technico, CramerKit, Shepardson Micro Systems, Cromenco, MicroPro, Ramtek, Oliver Audio, Inc., etc. Ultraviolet Erasure lights and fixtures are available from Ultraviolet Products, Turner Designs, and others.

NOTE: Information on EPROM programmers and erasurers are provided only for user convenience and do not indicate any preference by TI.

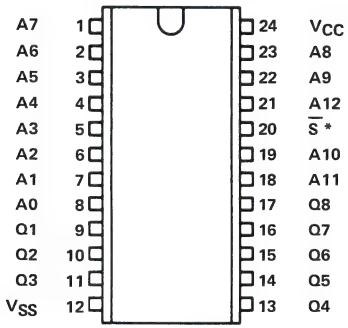
ROM DATA SHEETS

- TMS 4732 . . . 4096 X 8 Organization
- TMS 4764 . . . 8192 X 8 Organization
- All Inputs and Outputs TTL-Compatible
- Fully Static (No Clocks, No Refresh)
- Single 5-V Power Supply
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- 3-State Outputs for OR-Ties
- Pin-Compatible with TI's EPROM Family
- N-Channel Silicon-Gate Technology
- 8-Bit Output Ideal for Microprocessor Based Systems

TMS 4732
4K X 8 5V ROM
24-PIN
DUAL-IN-LINE PACKAGE



TMS 4764
8K X 8 5 V ROM
24-PIN**
DUAL-IN-LINE PACKAGE



* Option: Either $\overline{S}$ or Non-Clocked Chip Enable/Power Down ($\overline{E}$)

** Also available in 28-pin Dual-in-line package. Both 24-pin and 28-pin packages are compatible with TI 64K EPROMs.

description

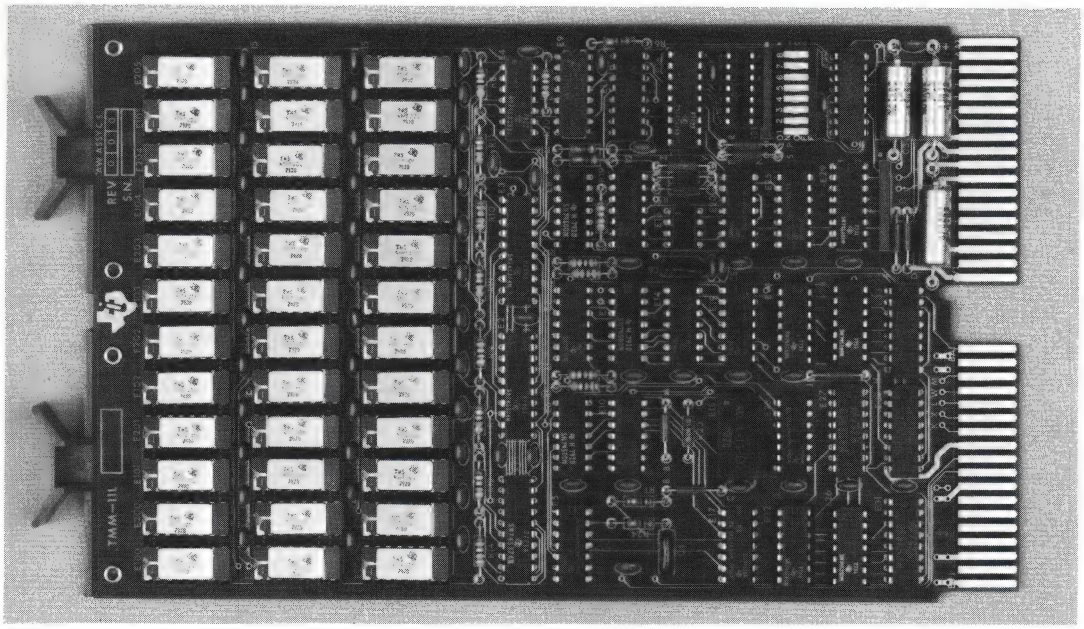
TI provides ROMs on a custom basis. Density options are 32K and 64K. Both devices are pin compatible with TI 32K and 64K 5 V ROMs and EPROMs. Any additional specifications should be made at the time of the order. For further information, contact a nearby sales office or write Texas Instruments, P. O. Box 1443, M/S 6965, Houston, Texas 77001.

MEMORY SYSTEMS DATA SHEETS

TMM 10000 SERIES
ADD-IN MEMORY FOR LSI-11 COMPUTERS

JANUARY 1980

- High Density: 64K Words X 18 Bits (for LSI-11/23), 32K Words X 18 Bits (for LSI-11/2)
- Completely Compatible with Q BUS and Q BUS PLUS Systems
- Extended Addressing to 1 Megabyte (Optional)
- Single 5-Volt Supply, Low Power Consumption
- Parity Logic on Board
- High Performance (with Parity Generation and Checking
- Internal, Transparent Refresh



description

The TMM 10000 Series add-in memory module is offered in two versions, each of which is compatible with the LSI-11 Q BUS and Q BUS PLUS system. The TMM 10103 module plugs directly into the DEC LSI-11/23 (PDP-11/23) computer; the TMM 10101 module plugs directly into the DEC LSI-11/2 (PDP-11/03) computer. All interface specifications are totally compatible. The modules use the TMS 4532 five-volt 32K dynamic RAM for high performance and low power. Both feature on-board parity logic.

NOTE: Q BUS, Q BUS PLUS, and DEC are trademarks of the Digital Equipment Corporation.

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ADVANCE INFORMATION

This document contains information on a new product. Specifications are subject to change without notice.

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TMM10000 SERIES
ADD-IN MEMORY FOR LSI-11 COMPUTERS

specifications

Memory Capacity:

MODEL NO.	WORDS	BITS/WORD
TMM-10103-18P	65,536	16 + 2 parity bits
TMM-10101-18P	32,368	16 + 2 parity bits

Timing:

Read Access	200 ns
Write Access	150 ns
Read/Write Cycle	450 ns

Power:

+5 V, 10.5 W Active
7.9 W Standby
5.25 W Battery back-up

Physical:

Single width, double height
(5.2" X 8.9")

Environmental, Operating:

5°C to 60°C
10% to 95% relative humidity, non-condensing

features

I/O Page Size	512, 2048, 3072, or 4096 words
Starting Address	Any 4K word boundary
Total Address Space*	128K words
Parity	Generated on board
Memory Refresh	Internal or external
Battery Back-Up	Enable with +5 V to pin AV1

*20 Address Lines are available for user expansion of system memory to 512K words.

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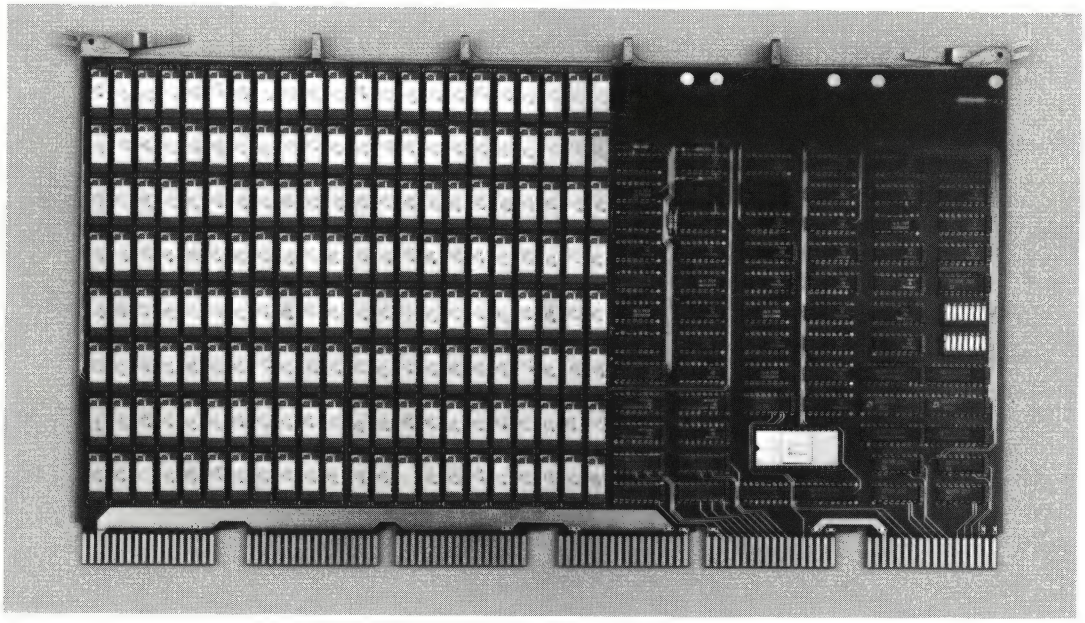
IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSI

TMM 20000 SERIES
ADD-IN MEMORY FOR PDP COMPUTERS

JANUARY 1980

- High Density . . . 256K, 128K, or 96K (16 Bit) Words, Plus 6 Bits for Error Detection and Correction
- Completely Compatible with PDP-11 UNIBUS (Modified or Extended) Systems
- Single-Bit Error Correction, Double-Bit Error Detection with Visual Display
- Twenty-two Address Lines Allow for Future Expansion to 2M Words
- Single +5-Volt Supply, Low Power Consumption
- Error Logging Capability Via User Program



description

The TMM 20000 Series add-in modules are fully compatible with the DEC PDP-11 family of UNIBUS computers. Employing the TMS 4532 32K Dynamic RAM, these modules offer high density and operate from a single five-volt power supply with low power consumption. These modules offer high speed, increased reliability, and error detection and correction, and are designed to allow direct upgrade to the TMS 4164 64K Dynamic RAM. Battery back-up is jumper selectable.

error detection and correction (EDAC)

On-board circuitry performs single-bit error correction and double-bit error detection. Control (CSR) and error (ESR) status registers, with single- and double-bit error display are standard. All error detection and correction operations are transparent to the operating system.

NOTE: UNIBUS and DEC are trademarks of the Digital Equipment Corporation.

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TMM 20000 SERIES
ADD-IN MEMORY FOR PDP COMPUTERS

specifications

Memory Capacity:

MODEL NO.	WORDS	BITS/WORD
TMM-20106-22E	262,144	22
TMM-20105-22E	131,072	22
TMM-20104-22E	98,304	22

Timing:

Read access	425 ns
Write access	200 ns
Read/write cycle	550 ns

Power:

+5 V, 20 W active; 12 W standby/backup

Physical:

Single width, hex height

Environmental, Operating:

0°C - 50°C; 10% - 95% Relative Humidity (Noncondensing)

programmable features

- Modified or extended UNIBUS: switch select
- I/O page size: 2K, 4K, or 8K words (switch select)
- Starting address (switch select): any 16K word boundary
- Total address space (switch select): modified UNIBUS - 128K words (256K bytes)
  extended UNIBUS- 2048K words (4M bytes)
- Control status register (CSR) address location (switch select): 1 of 16
- Error status register (ESR): on or off
- Battery backup: enable or disable (jumper)

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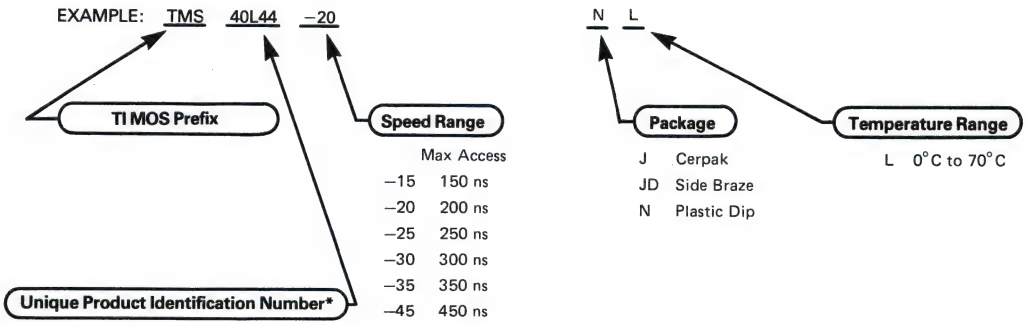
MECHANICAL DATA

general

Electrical characteristics presented in this catalog, unless otherwise noted, apply to device type(s) listed in the page heading, regardless of package. Factory orders for devices described should include the complete part-type numbers listed on each page.

MOS NUMBERING SYSTEM



manufacturing information

Die-attach is by standard gold silicon eutectic or by conductive polymer.

Thermal compression gold wire bonding is used on plastic packaged circuits. Typical bond strength is 5 grams. Bond strength is monitored on a lot-to-lot basis. Any preseal bond strength of less than 2 grams causes rejection of the entire lot of devices. On hermetic devices either thermal compression or ultrasonic wire bonding is used. All hermetic MOS LSI devices produced by TI are capable of withstanding 5×10^{-7} atm cc/sec inspection and may be screened to 5×10^{-8} atm cc/sec fine leak, if desired by the customer, for special applications.

All packages are capable of withstanding a shock of 3000 g. All packages are capable of passing a 20,000 g acceleration (centrifuge) test in the Y-axis. Pin strength is measured by a pin-shearing test. All pins are able to withstand the application of a force of 6 pounds at 45° in the peel-off direction.

dual-in-line packages

A pin-to-pin spacing of 100 mils (2.54 mm) has been selected for standard dual-in-line packages.

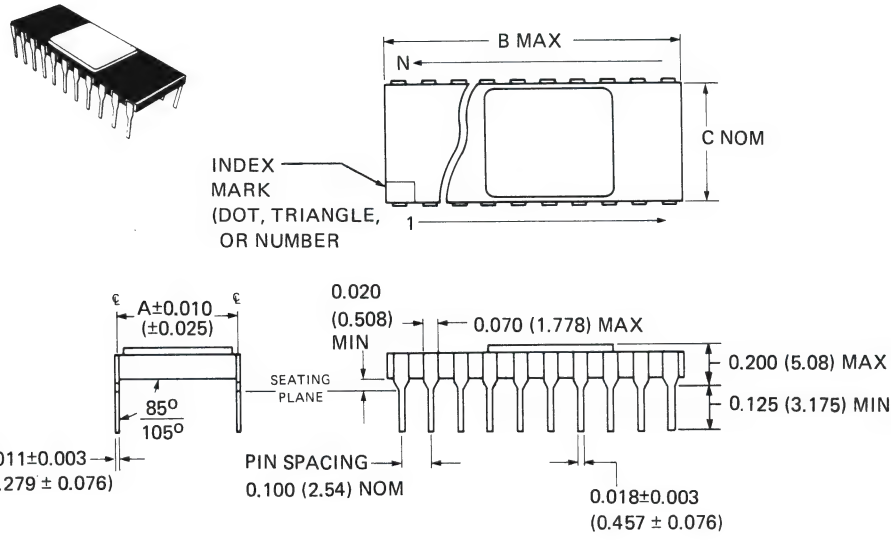
TI uses two basic types of hermetically sealed ceramic dual-in-line packages. The first type is the sidebrazed package cap and tin-plated leads. The second is the cerpak which is similar to the cerdip but has a clear or opaque lid above the bar.

* Inclusion of an "L" in the product identification indicates the device operates at low power.

MECHANICAL DATA

All measurements are given using both English and metric systems. Under the English system, the measurements are given in inches; under the metric system, the measurements are given in millimeters. The metric system measurements are indicated in parentheses next to the English.

ceramic packages — side braze (JD suffix)



DIM. \ PINS	16	18	20	22	24	28
A ± 0.010 (± 0.025)	0.300 (7.62)	0.300 (7.62)	0.300 (7.62)	0.400 (10.16)	0.600 (15.24)	0.600 (15.24)
B(MAX)	0.840 (21.34)	0.910 (23.11)	1.020 (25.91)	1.100 (27.94)	1.290 (32.77)	1.415 (35.94)
C(NOM)	0.295 (7.493)	0.295 (7.493)	0.295 (7.493)	0.395 (10.03)	0.595 (15.11)	0.595 (15.11)

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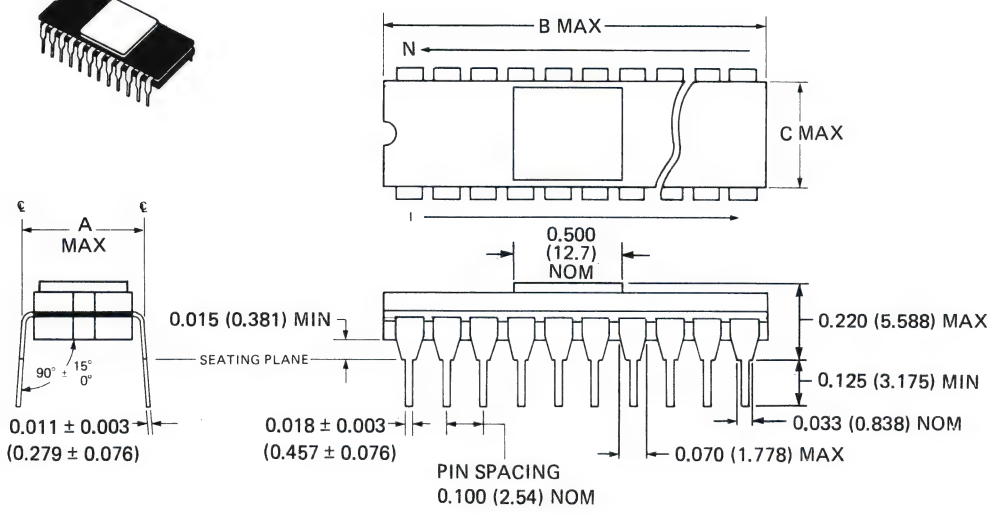
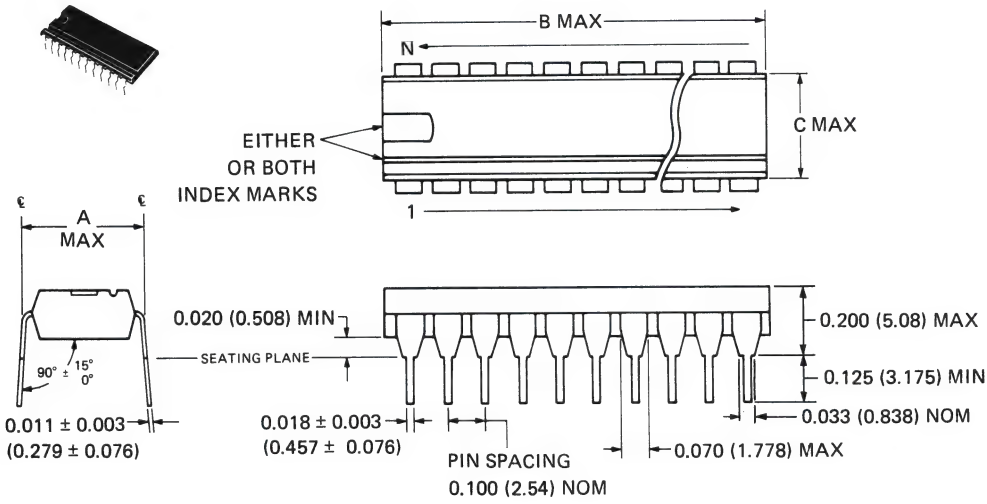
ceramic packages — cerpak (J suffix)



DIM. \ PINS	24	28
A (MAX)	0.625 (15.88)	0.625 (15.88)
B (MAX)	1.290 (32.77)	1.490 (37.85)
C (MAX)	0.600 (15.24)	0.600 (15.24)

plastic packages (N suffix)



DIM. \ PINS	16	18	20	22	24	28
A (MAX)	0.325 (8.255)	0.325 (8.255)	0.325 (8.255)	0.425 (10.80)	0.625 (15.88)	0.625 (15.88)
B (MAX)	0.870 (22.1)	0.920 (23.37)	1.070 (27.18)	1.120 (28.45)	1.270 (32.26)	1.440 (36.58)
C (MAX)	0.270 (6.858)	0.270 (6.858)	0.270 (6.858)	0.355 (9.017)	0.550 (13.97)	0.550 (13.97)

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MANUFACTURING FLOW

Standard Hermetic Processing Flow*

Slice Sawing
↓
Chip Inspection
↓
Chip Alloyed into Header
↓
Ultrasonic or Thermocompression Bond
↓
Preseal Inspection
↓
Seal
↓
Temperature Cycle (10 cycles at $-65^{\circ}C$ to $150^{\circ}C$)
↓
Centrifuge (20,000 G in Y1 direction)
↓
Tin Plate
↓
Fine Leak (5×10^{-8} atm cc/sec)
↓
Gross Leak (C_2 modified)
↓
Lead Tie-bar Sheared
↓
Testing
↓
Q/A Inspection
↓
Shipment

* For cerdip, cerpak, and sidebraze ceramic packages.

Standard Plastic Processing Flow

Slice Sawing
↓
Chip Inspection
↓
Chip Alloyed or Epoxied onto Leadframe
↓
Thermocompression Bond
↓
Premold Inspection
↓
Mold
↓
Tie-bar Sheared
↓
Testing
↓
Q/A Inspection
↓
Shipment

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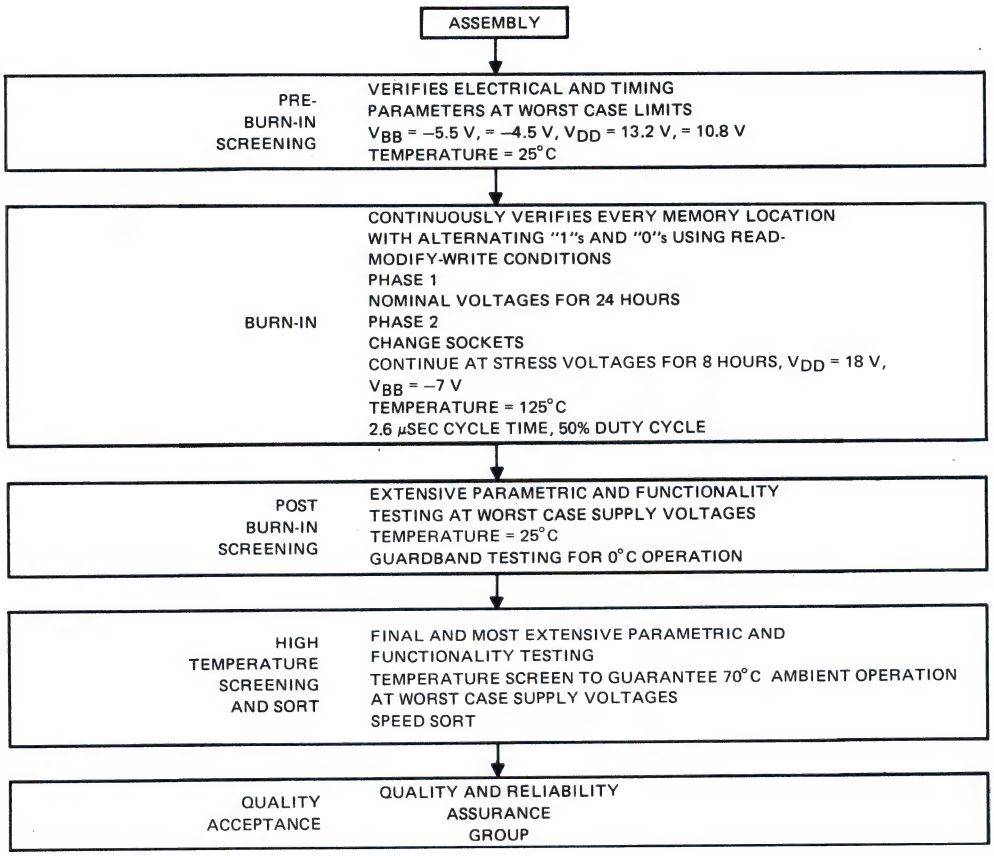
IN ORDER TO IMPROVE DESIGN AND TO SUPPLY THE BEST PRODUCT POSSIBL

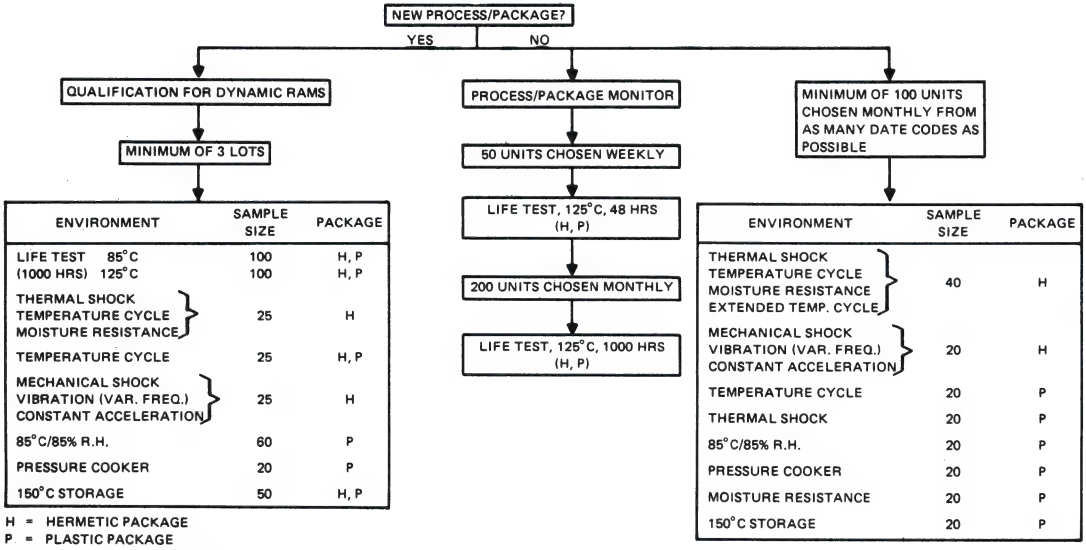
TESTING/RELIABILITY

In order to ensure the highest in quality and performance, each and every MOS memory device manufactured by the TI MOS Memory Division is thoroughly tested before being shipped. Testing is done during assembly by process engineering (indicated on the manufacturing flow in the previous section); After assembly by product engineering (final test); and after final test by quality and reliability assurance engineering. Every device is tested during the first two stages after which they are received by QRA for random screening for reliability. Outlines of the final test procedure and QRA screening process by family type are included in this section.

DYNAMIC RAMs – FINAL TEST


ASSEMBLY
PRE-BURN-IN SCREENING
VERIFIES ELECTRICAL AND TIMING PARAMETERS AT WORST CASE LIMITS
V_{BB} = –5.5 V, = –4.5 V, V_{DD} = 13.2 V, = 10.8 V
TEMPERATURE = 25°C
BURN-IN
CONTINUOUSLY VERIFIES EVERY MEMORY LOCATION WITH ALTERNATING "1"s AND "0"s USING READ-MODIFY-WRITE CONDITIONS
PHASE 1
NOMINAL VOLTAGES FOR 24 HOURS
PHASE 2
CHANGE SOCKETS
CONTINUE AT STRESS VOLTAGES FOR 8 HOURS, V_{DD} = 18 V, V_{BB} = –7 V
TEMPERATURE = 125°C
2.6 μSEC CYCLE TIME, 50% DUTY CYCLE
POST BURN-IN SCREENING
EXTENSIVE PARAMETRIC AND FUNCTIONALITY TESTING AT WORST CASE SUPPLY VOLTAGES
TEMPERATURE = 25°C
GUARDBAND TESTING FOR 0°C OPERATION
HIGH TEMPERATURE SCREENING AND SORT
FINAL AND MOST EXTENSIVE PARAMETRIC AND FUNCTIONALITY TESTING
TEMPERATURE SCREEN TO GUARANTEE 70°C AMBIENT OPERATION AT WORST CASE SUPPLY VOLTAGES
SPEED SORT
QUALITY ACCEPTANCE
QUALITY AND RELIABILITY ASSURANCE GROUP

DYNAMIC RAMs – QRA FLOW


NEW PROCESS/PACKAGE?
YES
NO
QUALIFICATION FOR DYNAMIC RAMS
MINIMUM OF 3 LOTS
PROCESS/PACKAGE MONITOR
50 UNITS CHOSEN WEEKLY
LIFE TEST, 125°C, 48 HRS (H, P)
200 UNITS CHOSEN MONTHLY
LIFE TEST, 125°C, 1000 HRS (H, P)
MINIMUM OF 100 UNITS CHOSEN MONTHLY FROM AS MANY DATE CODES AS POSSIBLE

ENVIRONMENT	SAMPLE SIZE	PACKAGE
LIFE TEST 85°C	100	H, P
(1000 HRS) 125°C	100	H, P
THERMAL SHOCK TEMPERATURE CYCLE MOISTURE RESISTANCE	25	H
TEMPERATURE CYCLE	25	H, P
MECHANICAL SHOCK VIBRATION (VAR. FREQ.) CONSTANT ACCELERATION	25	H
85°C/85% R.H.	60	P
PRESSURE COOKER	20	P
150°C STORAGE	50	H, P

H = HERMETIC PACKAGE
P = PLASTIC PACKAGE
ALL SELECTIONS ARE RANDOM
LIFE TEST UNITS ELECTRICALLY TESTED; PACKAGE ENVIRONMENTS FOLLOWED BY ELECTRICAL AND HERMETICITY (H ONLY) TESTS
(SEE MECHANICAL DATA SECTION)

ENVIRONMENT	SAMPLE SIZE	PACKAGE
THERMAL SHOCK TEMPERATURE CYCLE MOISTURE RESISTANCE EXTENDED TEMP. CYCLE	40	H
MECHANICAL SHOCK VIBRATION (VAR. FREQ.) CONSTANT ACCELERATION	20	H
TEMPERATURE CYCLE	20	P
THERMAL SHOCK	20	P
85°C/85% R.H.	20	P
PRESSURE COOKER	20	P
MOISTURE RESISTANCE	20	P
150°C STORAGE	20	P

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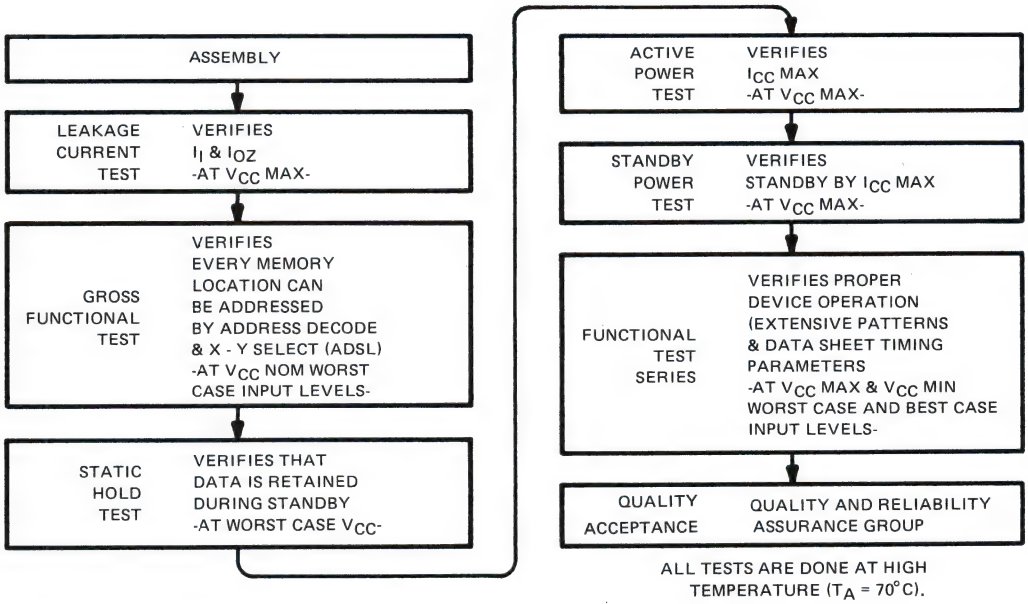
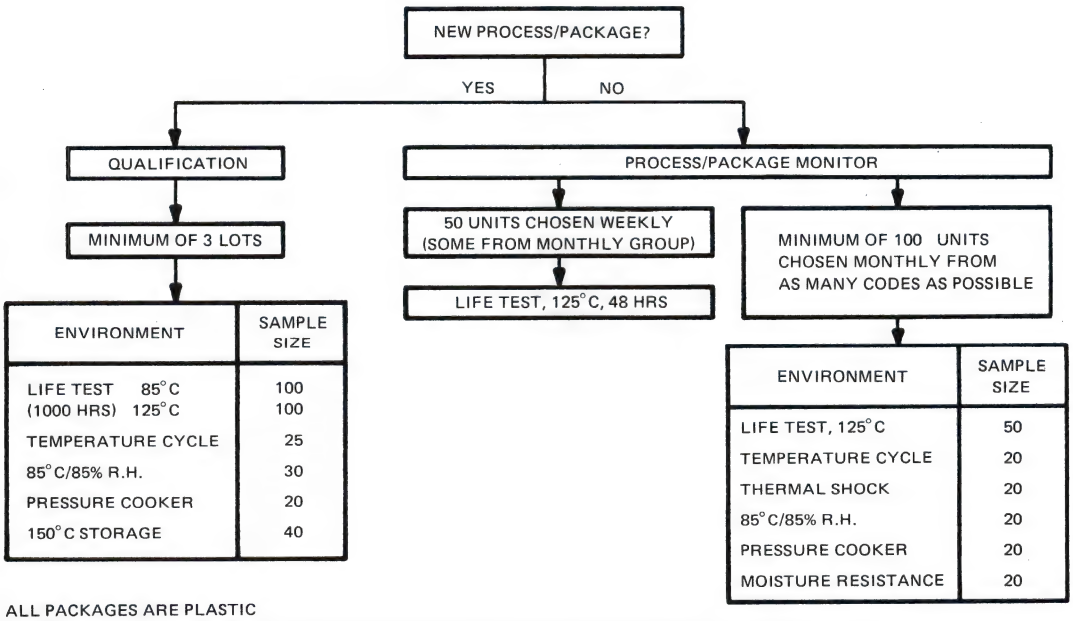
STATIC RAMs – FINAL TEST


ASSEMBLY
LEAKAGE CURRENT TEST
VERIFIES I_I & I_{OZ} -AT V_{CC} MAX-
GROSS FUNCTIONAL TEST
VERIFIES EVERY MEMORY LOCATION CAN BE ADDRESSED BY ADDRESS DECODE & X - Y SELECT (ADSL) -AT V_{CC} NOM WORST CASE INPUT LEVELS-
STATIC HOLD TEST
VERIFIES THAT DATA IS RETAINED DURING STANDBY -AT WORST CASE V_{CC}-
ACTIVE POWER TEST
VERIFIES I_{CC} MAX -AT V_{CC} MAX-
STANDBY POWER TEST
VERIFIES STANDBY BY I_{CC} MAX -AT V_{CC} MAX-
FUNCTIONAL TEST SERIES
VERIFIES PROPER DEVICE OPERATION (EXTENSIVE PATTERNS & DATA SHEET TIMING PARAMETERS -AT V_{CC} MAX & V_{CC} MIN WORST CASE AND BEST CASE INPUT LEVELS-
QUALITY ACCEPTANCE
QUALITY AND RELIABILITY ASSURANCE GROUP

ALL TESTS ARE DONE AT HIGH TEMPERATURE (T_A = 70°C).

STATIC RAMs – QRA FLOW

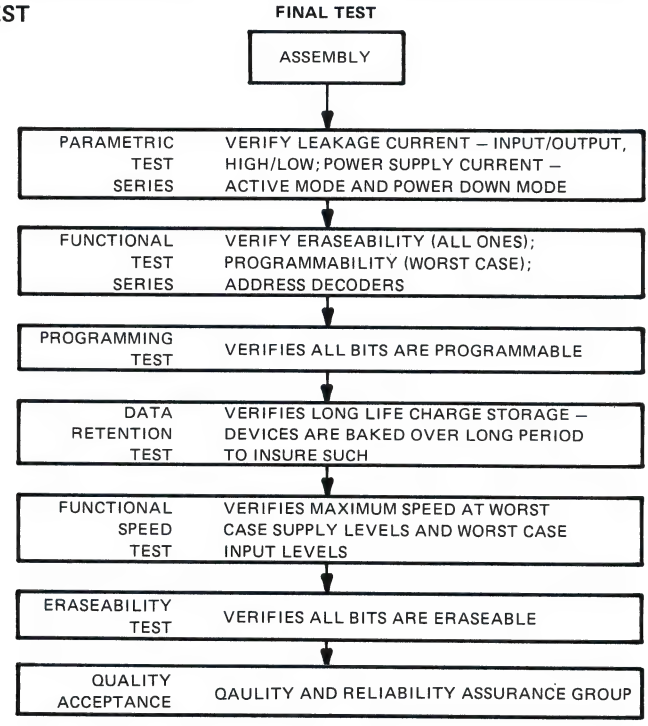

NEW PROCESS/PACKAGE?
YES
NO
QUALIFICATION
MINIMUM OF 3 LOTS
PROCESS/PACKAGE MONITOR
50 UNITS CHOSEN WEEKLY (SOME FROM MONTHLY GROUP)
LIFE TEST, 125°C, 48 HRS
MINIMUM OF 100 UNITS CHOSEN MONTHLY FROM AS MANY CODES AS POSSIBLE

ENVIRONMENT	SAMPLE SIZE
LIFE TEST 85°C (1000 HRS) 125°C	100 100
TEMPERATURE CYCLE	25
85°C/85% R.H.	30
PRESSURE COOKER	20
150°C STORAGE	40

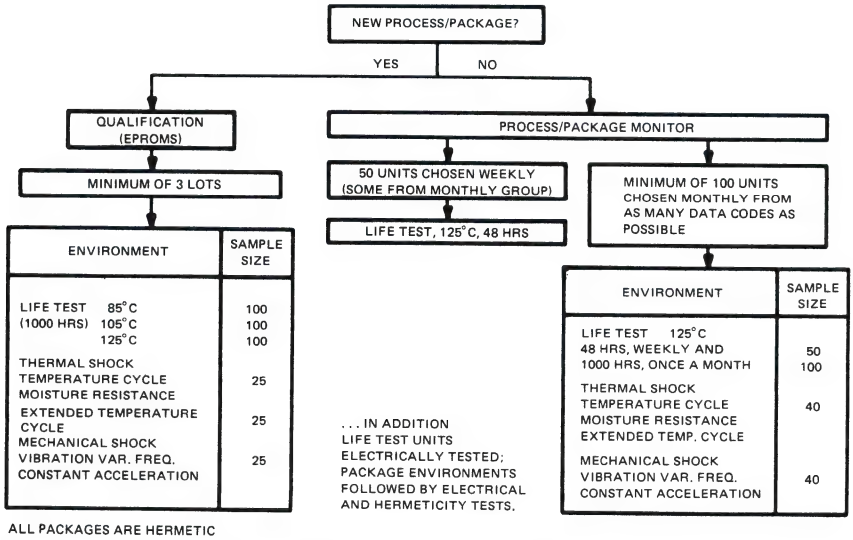
ENVIRONMENT	SAMPLE SIZE
LIFE TEST, 125°C	50
TEMPERATURE CYCLE	20
THERMAL SHOCK	20
85°C/85% R.H.	20
PRESSURE COOKER	20
MOISTURE RESISTANCE	20

ALL PACKAGES ARE PLASTIC
LIFE TEST UNITS ELECTRICALLY TESTED; PACKAGE ENVIRONMENTS FOLLOWED BY ELECTRICAL TESTS

EPROMs — FINAL TEST


FINAL TEST
ASSEMBLY
PARAMETRIC TEST SERIES
VERIFY LEAKAGE CURRENT — INPUT/OUTPUT, HIGH/LOW; POWER SUPPLY CURRENT — ACTIVE MODE AND POWER DOWN MODE
FUNCTIONAL TEST SERIES
VERIFY ERASEABILITY (ALL ONES); PROGRAMMABILITY (WORST CASE); ADDRESS DECODERS
PROGRAMMING TEST
VERIFIES ALL BITS ARE PROGRAMMABLE
DATA RETENTION TEST
VERIFIES LONG LIFE CHARGE STORAGE — DEVICES ARE BAKED OVER LONG PERIOD TO INSURE SUCH
FUNCTIONAL SPEED TEST
VERIFIES MAXIMUM SPEED AT WORST CASE SUPPLY LEVELS AND WORST CASE INPUT LEVELS
ERASEABILITY TEST
VERIFIES ALL BITS ARE ERASEABLE
QUALITY ACCEPTANCE
QAULITY AND RELIABILITY ASSURANCE GROUP

EPROMs — QRA FLOW



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GLOSSARY/TIMING CONVENTIONS/DATA SHEET STRUCTURE

PART I – GENERAL CONCEPTS AND TYPES OF MEMORIES

Address – Any given memory location to which data can be stored or retrieved.

Automatic Chip-Select/Power Down – (see Chip Enable Input)

Bit – Contraction of BInary digiT, e.e., a 1 or 0, in electrical terms a lack of or the presence of charge, voltage, or current.

Byte – A word of 8 bits (see word)

Chip Enable Input – A control input to an integrated circuit that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in a reduced-power standby mode.

Chip Select Input – Chip select inputs are gating inputs that control the input to and output from the memory. They may be of two kinds:

1. Synchronous – Clocked/latched with the memory clock. Affects the inputs and outputs for the duration of that memory cycle.
2. Asynchronous – Has direct asynchronous control of inputs and outputs. In the read mode, an asynchronous chip select functions like an output enable.

Column Address Strobe (CAS) – A clock used in dynamic RAMs to control the input of column addresses. It can be active high (CAS) or active low ($\overline{\text{CAS}}$).

Data – Any information stored or retrieved from a memory device.

Dynamic (Read/Write) Memory (DRAM) – A read/write memory in which the cells require the repetitive application of control signals in order to retain the stored data.

NOTES:
1. The words "read/write" may be omitted from the term when no misunderstanding will result.
2. Such repetitive application of the control signals is normally called a refresh operation.
3. A dynamic memory may use static addressing or sensing circuits.
4. This definition applies whether the control signals are generated inside or outside the integrated circuit.

Electrically Alterable Read-Only Memory (EAROM) – A nonvolatile memory that can be field-programmed like a PROM or EPROM, but that can be electrically erased by a combination of electrical signals at its inputs.

Erasable and Programmable Read-Only Memory (EPROM)/Reprogrammable Read-Only Memory – A field-programmable read-only memory that can have the data content of each memory cell altered more than once.

Erase – Typically associated with EPROMs and EAROMs. The procedure whereby programmed data is removed and the device returns to its unprogrammed state.

Field-Programmable Read-Only Memory – A read-only memory that after being manufactured, can have the data content of each memory cell altered.

Fixed Memory – A common term for ROMs, EPROMs, EAROMs, etc., containing data that is not normally changed. A more precise term for EPROMs and EAROMs is nonvolatile since their data may be easily changed.

Fully Static RAM – In a fully static RAM, the periphery as well as the memory array is fully static. The periphery is thus always active and ready to respond to input changes without the need for clocks. There is no precharge required for static periphery.

K – When used in the context of specifying a given number of bits of information, 1K = 2^{10} = 1024 bits. Thus, 64K = 64 X 1024 = 65,536 bits.

Large-Scale-Integration (LSI) – The description of any IC technology which enables condensing more than 100 equivalent gates onto a single chip.

Mask-Programmed Read-Only Memory — A read-only memory in which the data content of each cell is determined during manufacture by the use of a mask, the data content thereafter being unalterable.

Memory — A medium capable of storage of information from which the information can be retrieved.

Memory Cell — The smallest subdivision of a memory into which a unit of data has been or can be entered, in which it is or can be stored, and from which it can be retrieved.

Metal-Oxide Semiconductor (MOS) — The technology involving photolithographic layering of metal and oxide to produce a semiconductor device.

NMOS — A type of MOS technology in which the basic conduction mechanism is governed by electrons. (Short for N-channel MOS)

Nonvolatile Memory — A memory in which the data content is maintained whether the power supplied is connected or not.

Output Enable — A control input that, when true, permits data to appear at the memory output, and when false, causes the output to assume a high-impedance state. (See also chip select)

PMOS — A type of MOS technology in which the basic conduction mechanism is governed by holes. (Short for P-channel MOS)

Parallel Access — A feature of a memory by which all the bits of a byte or word are entered simultaneously at several inputs or retrieved simultaneously from several outputs.

Power Down — A mode of a memory device during which the device is operating in a low power or standby mode. Normally read or write operations of the memory are not possible under this condition.

Program — Typically associated with EPROM memories, the procedure whereby logical 0's (or 1's) are stored into various desired locations in a previously erased device.

Program Enable — An input signal that when true, puts a programmable memory device into the program mode.

Programmable Read-Only Memory (PROM) — A memory that permits access to any of its address locations in any desired sequence with similar access time to each location.
NOTE: The term as commonly used denotes a read/write memory.

Read — A memory operation whereby data is output from a desired address location.

Read-Only Memory (ROM) — A memory in which the contents are not intended to be altered during normal operation.
NOTE: Unless otherwise qualified, the term "read-only memory" implies that the content is determined by its structure and is unalterable.

Read/Write Memory — A memory in which each cell may be selected by applying appropriate electrical input signals and the stored data may be either (a) sensed at appropriate output terminals, or (b) changed in response to other similar electrical input signals.

Row Address Strobe (RAS) — A clock used in dynamic RAMs to control the input of the row addressed. It can be active high (RAS) or active low ($\overline{\text{RAS}}$).

Scaled-MOS (SMOS) — MOS technology under which the device is scaled down in size in three dimensions and in operating voltages allowing improved performance.

Semi-Static (Quasi-Static, Pseudo-Static) RAM — In a semi-static RAM, the periphery is clock-activated (i.e., dynamic). Thus the periphery is inactive until clocked, and only one memory cycle is permitted per clock. The peripheral circuitry must be allowed to reset after each active memory cycle for a minimum precharge time. No refresh is required.

Serial Access — A feature of a memory by which all the bits are entered sequentially at a single input or retrieved sequentially form a single output.

Static RAM (SRAM) — A read/write random-access device within which information is stored as latched voltage levels. The memory cell is a static latch that retains data as long as power is applied to the memory array. No refresh is required. The type of periphery circuitry sub-categorizes static RAMs.

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Very-Large-Scale-Integration (VLSI) — The description of any IC technology which enables condensing over 1,000 equivalent gates into a single chip.

Volatile Memory — A memory in which the data content is lost when power supplied is disconnected.

Word — A series of one or more bits that occupy a given address location and that can be stored and retrieved in parallel.

Write — A memory operation whereby data is written into a desired address location.

Write Enable — A control signal that when true causes the memory to assume the write mode, and when false causes it to assume the read mode.

PART II — OPERATING CONDITIONS AND CHARACTERISTICS (INCLUDING LETTER SYMBOLS)

The symbols for quantities involving time use upper and lower case letters according to the following historically evolved principles:

a. Time itself, is always represented by a lower case t.
b. Subscripts are lower case when one or more letters represent single words, e.g., d for delay, su for setup, rd for read, wr for write.
c. Multiple subscripts are upper case when each letter stands for a different word, e.g., CS for chip select, PLH for propagation delay low to high, RMW for read, modify, write.

Access Time

The time between the application of a specified input pulse during a read cycle and the availability of valid data signals at an output.

Example symbology:

$t_{a(ad,LH)}$	Access time from address, low-to-high-level output
$t_{a(ad,HL)}$	Access time from address, high-to-low-level output
$t_{a(CE)}$, $t_{a(E)}$	Access time from chip enable
$t_{a(CS)}$, $t_{a(S)}$	Access time from chip select

Capacitance

The inherent capacitance on every pin, which can vary with various inputs and outputs.

Example symbology:

C_i	Input capacitance
C_o	Output capacitance
$C_{i(D)}$	Input capacitance, data input

Current

High-level input current, I_{IH}
The current into an input when a high-level voltage is applied to that input.

High-level output current, I_{OH}
The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input current, I_{IL}
The current into an input when a low-level voltage is applied to that input.

Low-level output current, I_{OL}
The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

* Current out of a terminal is given as a negative value.

Off-state (high-impedance-state) output current (of a three-state output), I_{OZ}
The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

Short-circuit output current, I_{OS}
The current into* an output when the output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

Supply current I_{BB}, I_{CC}, I_{DD}, I_{PP}
The current into, respectively, the V_{BB}, V_{CC}, V_{DD}, V_{PP} supply terminals.

* Current out of a terminal is given as a negative value.

Cycle Time

Read cycle time, $t_{c(rd)}$ (See Note)
The time interval between the start and end of a read cycle.

Read-write cycle time, $t_{c(RW)}$ (or read-modify-write cycle time, $t_{c(RMW)}$ (See Note)
The time interval between the start of a cycle in which memory is read and new data is entered and the end of that cycle.

Write cycle time, $t_{c(wr)}$
The time interval between the start and end of a write cycle.

NOTE: A cycle time is the actual time between two intervals and may be insufficient for the completion of operations within the memory. A minimum value is specified that is the shortest time in which the memory will perform its read and/or write function correctly.

Data Valid Time

Data valid time with respect to chip select, $t_{DV(CS)}$
The interval following chip deselection during which output data continues to be valid.

Data valid time with respect to address, $t_{DV(ad)}$
The interval following an initial change of address during which data stored at the initial address continues to be valid at the output.

Delay Time

The time between the specified reference points on two waveforms.

Example symbology:

$t_{d(\phi 1 - \phi 2)}$	Delay time, clock 1 to clock 2
$t_{d(PH-CEH)}$	Delay time, precharge high to chip enable high
t_{RLCH}	Delay time, RAS going low to CAS going high (new symbology)

Hold Time

Hold time, t_h
The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

NOTES:
1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

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Example symbology:

$t_{h(ad)}$	Address hold time
$t_{h(da)}$	Data hold time
$t_{h(rd)}$	Read hold time
$t_{h(wr)}$	Write hold time
$t_{h(rs)}$	Reset hold time

Operating Free-Air Temperature

The temperature (T_A) range over which the device will operate and meet the specified electrical characteristics.

Output Enable and Disable Time

Output enable time (of a three-state output) to high level, t_{PZH} (or low level, t_{PZL})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

Output enable time (of a three-state output) to high or low level, t_{PZX}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

Output disable time (of a three-state output) from high level, t_{PHZ} (or low level, t_{PLZ})

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

Output disable time (of a three-state output) from high or low level, t_{PXZ}

The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

Propagation Time

Propagation delay time, t_{PD}

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

Propagation delay time, low-to-high-level output, t_{PLH}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

Propagation delay time, high-to-low-level output, t_{PHL}

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

Pulse Width

Pulse width, t_w

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

Example symbology:

$t_{w(CEH)}$	Pulse width, chip enable high
$t_{w(CEL)}$	Pulse width, chip enable low
$t_{w(clr)}$	Clear pulse width
$t_{w(CS)}$	Chip-select pulse width
$t_{w(\phi)}$	Clock pulse width
$t_{w(rs)}$	Reset pulse width
$t_{w(wr)}$	Write pulse width

Refresh Time Interval

Refresh time interval, $t_{refresh}$ (or t_{REF})

The time interval between the beginnings of successive signals that are intended to restore the level in a dynamic memory cell to its original level.

NOTE: The refresh time interval is the actual time between two refresh operations and may be insufficient to protect the stored data. A maximum value is specified that is the longest interval for which correct operation is guaranteed.

Setup Time

Setup time, t_{su}

The time interval between the application of a signal that is maintained at a specific input terminal and a specified subsequent active transition at another specified input terminal.

NOTES:
1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. Minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.
2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

Example symbology:

$t_{su(ad)}$	Address setup time
$t_{su(da)}$	Data setup time
$t_{su(rd)}$	Read setup time
$t_{su(wr)}$	Write setup time

Transition Time

Transition time, low-to-high-level, t_{TLH}

The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level. Also known as rise time, t_r.

Transition time, high-to-low-level, t_{THL}

The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level. Also known as fall time, t_f.

Voltage

High-level input voltage, V_{IH}

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

NOTE: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

High-level output voltage, V_{OH}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

Low-level input voltage, V_{IL}

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

NOTE: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

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Low-level output voltage, V_{OL}

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

Supply Voltages, V_{BB}, V_{CC}, V_{DD}, V_{PP}

The voltages supplied to the corresponding voltage pins that are required for the device to function. From one to four of these supplies may be necessary, along with ground, V_{SS}.

PART III – TIMING DIAGRAMS CONVENTIONS

TIMING DIAGRAM SYMBOL	MEANING	
	INPUT FORCING FUNCTIONS	OUTPUT RESPONSE FUNCTIONS
	Must be steady high or low	Will be steady high or low
	High-to-low changes permitted	Will be changing from high to low sometime during designated interval
	Low-to-high changes permitted	Will be changing from low to high sometime during designated interval
	Don't Care	State unknown or changing
	(Does not apply)	Center line is high-impedance off-state

PART IV – BASIC DATA SHEET STRUCTURE

The front page of the data sheet begins with a list of key *features* such as organization, interface, compatibility, operation (static or dynamic), access and cycle times, technology (N or P channel, silicon or metal oxide gate), and power. In addition, the top view of the device is shown with the *pinout* provided. Next a general *description* of the device, system interface considerations, and elaboration on other device characteristics are presented. The next section is an explanation of the device's *operation* which includes the function of each pin (i.e., the relationship between each input (output) and a given type of memory). The functions basically involve starting, achieving, and ending a given type of memory cycle (e.g., programming or erasing EPROMs, or reading a memory location).

Usually the next few pages contains the *absolute maximum ratings* (e.g., voltage supplies, voltage input, and temperature) over the *operating free-air temperature range*. If the device is used outside of these values, it may be permanently destroyed or at least it would not function as intended. Following this table is usally a *functional block diagram*, a flow chart of the basic internal structure of the device showing the signal paths for data, addresses, and control signals, as well as the internal architecture. Next, typically, are the *recommended operating conditions* (e.g., supply voltages, input voltages, and operating temperature). The memory device is guaranteed to work reliably and to meet all data sheet parameters when operated in accord with the recommended operating conditions and within the specified timing. If the device is operated outside of these limits (minimum/maximum), the device's operation is no longer guaranteed to meet the data sheet parameters. Operation beyond the absolute maximum ratings as just described can result in catastrophic failures.

The next section provides a table of *electrical characteristics over full ranges of recommended operating conditions* (e.g., input and output currents, output voltages, etc.). These are presented as minimum, typical, and maximum values. Typical values are representative of operation at an ambient temperature of $T_A = 25^\circ C$ with all power supply voltages at nominal value. Next, input and output capacitances are presented. Each pin has a capacitance (whether an input, an output, or control pin). Minimum capacitances are not given, as the typical and maximum values are the most crucial.

The next few tables involve the device timing characteristics. The parameters are presented as minimum, typical (or nominal), and maximum. The *timing requirements over recommended supply voltage range and operating free-air temperature* indicate the device control requirements such as hold times, setup times, and transition times. These values are referenced to the relative positioning of signals on the timing diagrams, which follow. The *switching characteristics over recommended supply voltage range* are device performance characteristics inherent to device operation once the inputs are applied. These parameters are guaranteed for the test conditions given. The interrelationship of the timing requirements to the switching characteristics is illustrated in *timing diagrams* for each type of memory cycle (e.g., read, write, program).

At the end of a data sheet additional *applications information* may be provided such as how to use the device, graphs of electrical characteristics, or other data on electrical characteristics.

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LOGIC SYMBOLS

EXPLANATION OF NEW LOGIC SYMBOLS FOR MEMORIES

1.0 INTRODUCTION

The International Electrotechnical Commission (IEC) has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic circuit to each output without showing explicitly the internal logic. At the heart of the system is dependency notation, which will be partially explained below.

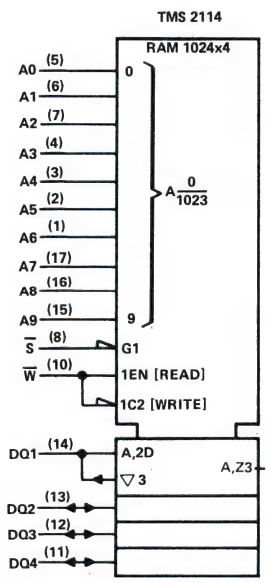
The system was introduced in the USA in a rudimentary form in IEEE/ANSI Standard Y32.14-1973. Lacking at that time a complete development of dependency notation, it offered little more than a substitution of rectangular shapes for the familiar distinctive shapes for representing the basic functions of AND, OR, negation, etc. This is no longer the case.

Internationally, Working Group 2 of IEC Technical Committee TC-3 is preparing a new document (Publication 617-12) that will consolidate the original work started in the mid 1960's and published in 1972 (Publication 117-15) and the amendments and supplements that have followed. Similarly for the USA, IEEE Committee SCC 11.9 is revising the publication IEEE Std 91/ANSI Y32.14. Texas Instruments is participating in the work of both organizations and this 1980 Edition of the MOS Memory Data Book introduces new logic symbols in anticipation of the new standards. When changes are made as the standards develop, future editions of this book will take those changes into account. Unfortunately, time and publication schedules have prevented the preparation of symbols for all the devices. This work will continue.

The following explanation of the new symbolic language is necessarily brief and greatly condensed from what the standards publications will finally contain. This is not intended to be sufficient for those people who will be developing symbols for new devices. It is primarily intended to make possible the understanding of the symbols used in this book.

2.0 EXPLANATION OF A TYPICAL SYMBOL

The TMS 2114 symbol will be explained in detail. This symbol includes almost all the features found in the others. Section 3.0, Diagramatic Summary, should be referred to while reading this explanation.



By convention all input lines are located on the left and output lines are located on the right. When an exception is made, an arrowhead shows reverse signal flow. The input/output lines (DQ1 through DQ4) illustrate this.

The polarity indicator ◺ indicates that the external low level causes the internal 1 state (the active state) at an input or that the internal 1 state causes the external low level at an output. The effect is similar to specifying positive logic and using the negation symbol ○ .

The rest of this discussion concerns features inside the symbol outline. The address inputs are arranged in the order of their assigned binary weights and the range of the addresses are shown as A-$\frac{m}{n}$ where m is the decimal equivalent of the lowest address and n is the highest. The inputs and outputs affected by these addresses are designated by the letter A.

The letter Z followed by a number is used to transfer a signal from one point in a symbol to another. Here the signal at output A,Z3 transfers to the 3 at the left side of the symbol in order to form an input/output port. The A means the output comes from the storage location selected by the address inputs.

The ▽ symbol designates a three-state output. Three-state outputs will always be controlled by an EN function. When EN stands at its internal 1 state, the outputs are enabled. When EN stands at its internal 0 state, the three-state outputs stand at their high-impedance states.

Since the boxes associated with DQ2, DQ3, and DQ4 have no internal qualifying symbols, it is to be understood that these boxes are identical to the box associated with DQ1.

Any D input is associated with storage. Whatever internal state is taken on by the D input is stored. The letter A (in A,Z3) indicates that the state of the D input will be stored in a cell selected by the A inputs. If the D input is disabled, the storage element retains its content.

Various types of relationships between ports can be indicated by what is called dependency notation. A letter indicating the type of dependency (e.g., C, G, Z) is placed at the affecting input (or output) and this is followed by a number. Each affected input (or output) is labeled with that same number. The Z symbol explained above is one form of dependency notation. Several other types of dependency have been defined but their use has not been anticipated in this book.

The numeral 2 at the D input indicates that the D input is affected by another input, in this case a C input (i.e., 1C2). When a C input stands at its internal 1 state, it enables the affected D input(s). When the C input stands at its internal 0 state, it disables the D input(s) so that it (they) can no longer alter the contents of the storage element(s).

The C input is itself affected by another input. The numeral 1 in front of the C shows that a dependency relationship exists with a G input. The letter G indicates an AND relationship. When a G input stands at its internal 1 state (low in this case), the affected inputs (EN and C2 here) are enabled. When the G input stands at its internal 0 state, it imposes the 0 state on the affected inputs.

Pin 10 has two functions. Its function as a C input has just been explained. Note that for the C input function to stand at its 1 state, pin 10 must be low and pin 8 must also be low. The other function of pin 10 is as an EN input. This controls the 3-state outputs. This EN input is also affected by the AND relationship with pin 8 so for the EN function to stand at its internal 1 state (enabling the outputs), pin 10 must be high and pin 8 must be low.

Labels within square brackets are merely supplementary and should be self-explanatory.

If you have questions on this Explanation of New Logic Symbols, please contact:

F. A. Mann MS84
Texas Instruments Incorporated
P.O. Box 225012
Dallas, Texas 75265
Telephone (214) 238-3746

IEEE Standards may be purchased from:

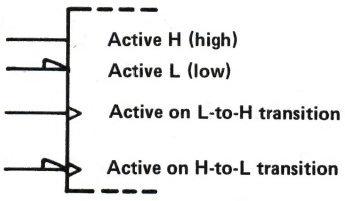
Institute of Electrical and Electronics Engineers, Inc.
345 East 47th Street
New York, N.Y. 10017

International Electrotechnical Commission (IEC) publications may be purchased from:

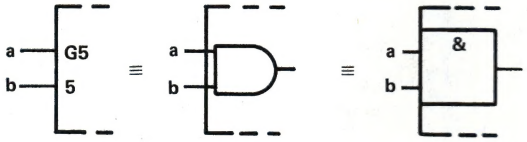
American National Standards Institute, Inc.
1430 Broadway
New York, N.Y. 10018

DIAGRAMATIC SUMMARY

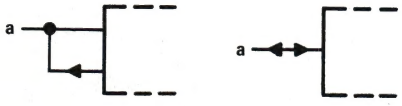
INPUTS



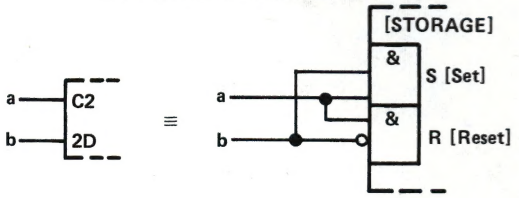
G (AND) DEPENDENCY



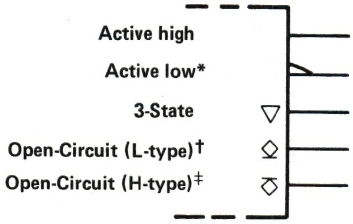
INPUT/OUTPUT



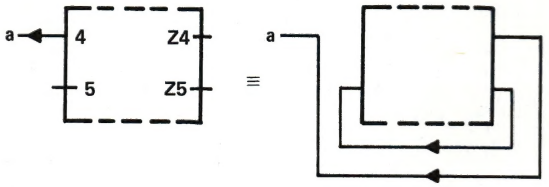
C (CONTROL) DEPENDENCY



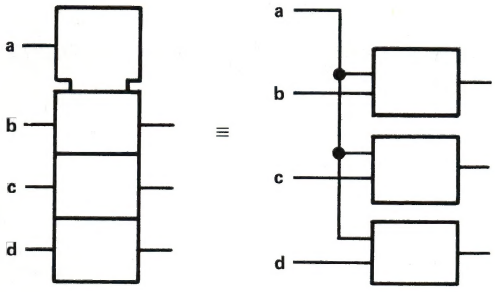
OUTPUTS



Z (INTERCONNECTION) DEPENDENCY



COMMON CONTROL BLOCK



* The active-low indicator may be used in combination with the 3-state and open-circuit indicators.

† L-types include N-channel open-drain and P-channel open-source outputs.

‡ H-types include P-channel open-drain and N-channel open-source outputs.

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